Wednesday, April 19

	Room A	Room B	Room C	Room D	Room E
9:30 11:10	**WA1: iNEMI Session** Chairs: Y. Tomita, Intel, M. Fujino, AIST **WA1-1** Preparing for 6G: Developing Best Practices and Standards for Industrial Measurements of Low-Loss Dielectrics Lucas Enright[1], Marzena Olszewska-Placha[2], Michael Hill[3], Say Phommakesone[4], Daisuke Kato[4], Charles A. Hill[5], Hanna Kahari[6], Chiawen Lee[7], Chang-Sheng Chen[7], Nathan D. Orloff[1], Malgorzata Celuch[2], Urmi Ray[8], [1]National Institute of Standards and Technology / USA, [2]QWED / Poland, [3]Intel, [4]Keysight Technologies, [5]3M / USA, [6]Nokia / Finland, [7]Industrial Technology Research Institute / Taiwan, [8]International Electronics Manufacturing Initiative / USA **WA1-2** AOI Pattern Detection Study for Fine Pitch Advanced Substrate Feng Xue[1], Zhihua Zou[2], Charles Reynolds[1], Tom Wassick[1], Glenn Pomerantz[1], Neil Tang[3], ChaoLin Cheng[4], Steven Martell[5], Masahiro Tsuriya[6], [1]IBM / USA, [2]Intel / USA, [3]AT&S / China, [4]Unimicron / Taiwan, [5]Nordson Test & Inspection / USA, [6]International Electronics Manufacturing Initiative / Japan **WA1-3** Copper Trace Adhesion Measurement Study for Advanced Substrate Circuitry Patterns Lisa Y. Chen[1], Tzu-Hsuan Wang[2], Yanchun Deng[3], Iqbal Mokhtar[4], Steven R. Martell[5], Masahiro Tsuriya[6], [1]Intel / USA, [2]Unimicron Technology / Taiwan, [3]AT&S (Chongqing) / China, [4]Intel / Malaysia, [5]Nordson T&I / USA, [6]International Electronics Manufacturing Initiative / Japan **WA1-4** An In-containing Lower-Temperature Lead-Free Solder Paste for Wafer-Level Package Application that Outperforms SAC305 HongWen Zhang, Sze Pei Lim, Indium / USA	**WB1: Advanced Packaging-1** Chairs: F. Inoue, Yokohama National Univ., M. Nakazawa, Sony Semiconductor Solutions **WB1-1** Selective Cu Surface Activation for Cu-Sn Thermocompression Bonding without Flux Deposition Ryo Negishi, Satoshi Saito, Itsuro Tomatsu, MEC / Japan **WB1-2** Hybrid Surface Treatment for Copper-to-Copper Thermal Compression Bonding Liang-Hsing Shih[1], Wei-Ting Chen[1], Viktor Lin[2], Jenn-Ming Song[1], [1]National Chung Hsing University, [2]Advanced Semiconductor Engineering Group / Taiwan **WB1-3** Fabrication of Highly (111)-oriented Nanotwinned Cu in Fine-pitch Vias for Cu/SiO_2 Hybrid Bonding Shih-Chi Yang[1,2], Jia-Juen Ong[1,2], Dinh-Phuc Tran[1,2], Wei-Lan Chiu[3], Ou-Hsing Lee[3], Chia-Wen Chiang[3], Hsiang-Hung Chang[3], Chin-Hung Wang[3], Chih Chen[1,2], [1]National Chiao Tung University, [2]National Yang Ming Chiao Tung University, [3]Industrial Technology Research Institute / Taiwan **WB1-4** Fine-pitch <111>-oriented NT-Cu/SiO_2 Hybrid Joints with High Thermal Fatigue Resistance and Low Contact Resistivity Jia-Juen Ong[1], Wei-Lan Chiu[2], Hsiang-Hung Chang[2], Dinh-Phuc Tran[1], Chih Chen[1], [1]National Yang Ming Chiao Tung University, [2]Industrial Technology Research Institute / Taiwan	**WC1: DMR-Electrical** Chairs: F. Uchikoba, Nihon Univ., K. Hasegawa, JSR **WC1-1** Interconnect Table Description for Efficient 2.5/3D Design Omer Vikinski[1], Alexander Waizman[2], [1]Intel / Israel, [2]Intel / USA **WC1-2** Measurement of Thermal Strain of Metallized Silicon Nitride Substrate in Thermal Cycling Test by Digital Image Correlation Method Minh Chu Ngo, Hiroyuki Miyazaki, Kiyoshi Hirao, Manabu Fukushima, National Institute of Advanced Industrial Science and Technology / Japan **WC1-3** Semiconductor Package Design Flow and Platform Applied on Fan-out Chip on Substrate Youle Lin, Keng-Tuan Chang, Hung-Chun Kuo, Chih-Yi Huang, Chen-Chao Wang, Advanced Semiconductor Engineering / Taiwan **WC1-4** 3D Modeling Methodology For High-Speed Channels Transition Desmond Tan Hai Peng[1], Sivalingam Thirubalan[2], Suresh Kumar Kopparti[3], [1]ANSYS / Singapore, [2]FMicrochip Technology / India, [3]Microchip Technology / India	**WD1: Bonding Process & Mechanism** Chairs: S. Takyu, LINTEC, G. Hamasaka, Tokuyama **WD1-1** Failure Analysis of Joints Bonded by Ag-In Transient Liquid Phase Process During Shear Test Xunda Liu, Hiroaki Tatsumi, Zhi Jin, Hiroshi Nishikawa, Osaka University / Japan **WD1-2** Controlling Porosity during Transient Liquid Phase Bonding for High-Temperature Soldering Processes Nurul R. Abdul Razak[1,2], Xin F. Tan[1,3], Stuart D. McDonald[1], Michael J. Bermingham[1], Jeffery Venezuela[1], Tetsuro Nishimura[4], Kazuhiro Nogita[1], [1]The University of Queensland / Australia, [2]Universiti Malaysia Perlis / Malaysia, [3]Kyushu University, [4]Nihon Superior / Japan **WD1-3** Enhanced Cu-to-Cu Bonding by Using Sn Passivation Layer P. Y. Kung[1], W. L. Huang[1], C. L. Kao[2], Y. C. Hung[2], C. R. Kao[1], [1]National Taiwan University, [2]Advanced Semiconductor Engineering Group / Taiwan **WD1-4** Effects of Surface Contaminants on Bonding Strength for Direct Cu-Cu Bonding With Passivation Layer Alaric-Yohei Kawai Petillot[1], Shuichi Shoji[1], Hiroshi Kawarada[1], Jun Mizuno[1,3], [1]Waseda University / Japan, [2]National Cheng Kung University / Taiwan	**WE1: DPS Session** Chairs: Y. Morikawa, ULVAC, K. Takeuchi, Tohoku Univ. **WE1-1 <Session Invited>** Plasma Etching Technology in FEOL of Logic Device Masaru Izawa, Hitachi High-Tech / Japan **WE1-2 <Session Invited>** Reactive Ion Etching Challenges and Technology for Memory Device Fabrication S. Tahara, Tokyo Electron Miyagi / Japan **WE1-3 <Session Invited>** Challenges in High-Aspect-Ratio Hole Etching for 3D Flash Memory Manufacturing Mitsuhiro Omura, KIOXIA / Japan **WE1-4 <Session Invited>** Batch Type Chemical Dry Etching System Using HF Gas for 3D NAND Flash Memory Atsuaki Hashimoto, ULVAC / Japan
11:10 11:20	**Break**				
11:20 12:20	**Keynote Lecture I:** History, Achievement, Challenge, and Future Trend of IC Packaging Industry in China Tianchun Ye, Institute of Microelectronics of the Chinese Academy of Sciences Chairs: M. Fujino, AIST, J. Wang, Meisei Univ.				
12:20 13:10	**Lunch**				
13:10 14:00	**Award Ceremony**				
14:00 14:10	**Break**				
14:10 15:10	**Keynote Lecture II:** Evolution and Innovation of Silicon Island Kyushu (in Japanese) Hideyuki Okano, Kyushu Economic Research Center Chairs: A. Shigetou, NIMS, M. Aoyagi, Kumamoto Univ.				
15:10 16:00	**Break / Poster Session**				
16:00 17:00	**Keynote Lecture III:** Semiconductor Market Outlook and TSMC Introduction Makoto Onodera, TSMC Japan Chairs: S. Takyu, LINTEC, T. Aoki, IBM Japan				
17:00 18:30	**Kumamoto Catsle Free Visit**				
18:30 20:30	**Welcome Reception**				

■Poster Session

Poster sessions will be held from 15:10-16:00 on April 19 and from 16:10-16:50 on April 20.

PSI	Special Video Lecture <Session Invited> The Perspective of LED Lighting's Future Akari-Lisa Ishii, I.C.O.N. / Japan
P01	Reserch of Unknown Noise Source in Package Power Distribution System Wei-Chiao Wang[1], Hsing-Chuan Peng[1], Yu-Cong Wang[1], Chia-Lin Hsieh[1], Sung-Mao Wu[1], Ming-Shan Lin[2], Yuan-Fu Ku[3], [1]National University of Kaohsiung, [2]Bureau of Standards, Metrology and Inspection, [3]Taiwan testing and certification center / Taiwan
P02	Direct Cu Electroplating on CoWB Electroless Barrier Layer Shaohan Chen, Naoya Shiraiwa, Ryota Saida, Tomohiro Shimizu, Takeshi Ito, Shoso Shingubara, Kansai University / Japan
P03	Stress Relaxation Structure Using NI Nano-Particle/Al Micro-Particle Composite Paste for Power Device Packaging Y. Tanaka, Y. Kitaguchi, K. Koshiba, T. Iizuka, K. Tatsumi, Waseda University / Japan
P04	Adhesive Strength and Diffusion at Interfaces between Sintered Cu Layer and Metal Surfaces (Cu, Ag, Au, Pd, Pt, Ni, NiP_x, and NiB_x) Dai Ishikawa[1], Hideo Nakako[1], Thomas Blank[2], Helge Wurst[2], Felix Steiner[2], [1]Resonac / Japan, [2]Karlsruhe Institute of Technology / Germany
P05	Stress and Reliability of Underfills in Heterogeneous Integration Fan-Out Multichip Module Packages Wen-Yu Teng, Jackson Lee, Liang-Yih Hung, Don-Son Jiang, Yu-Po Wang, Siliconware Precision Industries / Taiwan
P06	Interconnection Properties of Epoxy-based Conductive Adhesives by Chemically Controlled Sintering of Silver Micro-fillers Takanori Fukushima, Masahiro Inoue, Gunma University / Japan
P07	Die Bond Track Copper Debris Formation Mechanism Study Wang Yue[1], Wang Haiyan[2], Chen YanTao[1], Deng Yong[1], [1]Leshan-Phoenix Semiconductor, [2]SH Electronics ChengDu / China
P08	The Effect of TEOS Ratio and Calcination Temperature on Photoluminescence of Electrospun Luminescent Fibers Y. C. Chao, J. Y. Shih, C. L. Chung, I-SHOU University / Taiwan
P09	Fabrication of Various Types of Si-Ti Fibers or Films by Electrospinning and Heat Treatment YI. MIN, LIN, CHANG. SHIUE. YU, C. L. CHUNG, I-SHOU University / Taiwan
P10	Effects of Temperature and Humidity on The Surface and Mechanical Properties of Beta-chitin/PCL Nanofibers Prepared by Electrospinning C. Y. TSAI, K. H. WU, C. L. CHUNG, I-SHOU University / Taiwan
P11	Change in Electrical Behavior of Stretchable Wires Printed on a Polyurethane-based Substrate Depending on Tensile Strain Rintaroh Yamamoto, Masahiro Inoue, Gunma University / Japan
P12	Rapid Silver Sinter Joining Technology for Large Area Chips Luobin Zhang[1,2], Chuantong Chen[1], Fupeng Huo[1], Wangyun Li[1], Katsuaki Suganuma[1], [1]Osaka University / Japan, [2]Harbin Institute of Technology (Shenzhen) / China
P13	Molecular Design of Amine-Based Surfactants for Improving Electrical Reliability of Copper-Filled Conductive Pastes Daisuke Otajima, Yukari Matsunami, Masahiro Inoue, Gunma University / Japan
P14	Global/Local Modeling Nickel-Gold Plating Process in PCB Manufacturing for Analysis of Plating Thickness Distribution Yu-Kuan Yeh, Yuan Yao, National Tsing Hua University / Taiwan
P15	Investigation of Solder Resist Opening Uniformity on Flip Chip Substrate Yuan-Chang Ni, Wen-Yu Teng, Yu-Cheng Pai, Carl Chen, Yu-Po Wang, Siliconware Precision Industries / Taiwan
P16	In Situ Kinetic Analysis for Ion Transport in Solid-Electrodeposition(SED) Process Shunsuke Yamada, Yohei Takashima, Takaaki Tsuruoka, Kensuke Akamatsu, Konan University / Japan
P17	Verification of Circuit Signal Detection Method for Non-contact Measurement System Min-Jun Guo[1], Shu-Yu Lin[1], Yu-Cong Wang[1], Chia-Lin Hsieh[1], Sung-Mao Wu[1], Shang-Chih Chou[2], [1]Micro Electronic Packaging Laboratory, [2]Taiwan Textile Research Institute / Taiwan
P18	Optimizing Activation Process for Strong Direct Bonding Between Diamond and Si Substrates S. Okita[1,2], T. Matsumae[2], Y. Kurashima[2], H. Takagi[2], H. Umezawa[2], M. Hayase[1], [1]Tokyo University of ScienceChiba, [2]National Institute of Advanced Industrial Science and Technology / Japan
P19	High Thermal Conductive Composite Resin Filled with Spherical and Polyhedral Aluminum Nitrides Takefumi Iida, Atsushi Sakamoto, Isao Masada, Saiko Fujii, Go Hamasaka, Teruhiko Nawata, Tokuyama / Japan
P20	Post-Buckling Analysis for Addressing Asymmetric Warping of Fan-Out Reconstitution Process Chia-Yu Chen[1], Yu-Ching Lee[1], Kuo-Shen Chen[1], Dao-Long Chen[2], Yu-Xuan Lin[2], Wei-Hong Lai[2], Hung-Chun Yang[1,2], Tang-Yuan Chen[2], Ching-Jenq Ho[1], Chin-Li Kao[2], [1]National Cheng-Kung University, [2]Advanced Semiconductor Engineering / Taiwan
P21	Analytical Study on Stress and Strain of Power Chip Laminated Structure Luan X.H.[1], Ding L.G.[2], Li X.M.[2], Zhang H.J.[2], Li K.W.[2], Zhou L.Z.[1], Wu F.S.[1], [1]Huazhong University of Science and Technology, [2]Chengdu perfect technology / China
P22	Electronic Packaging Interfacial Strength Measurement and Delamination Investigation Meng-Kai Shih[1], Yu-Hao Liu[1], Guan-Sian Lin[1], Eddie Hsu[2], Jonny Yang[2], [1]National Formosa University, [2]Richtek Technology / Taiwan

Thursday, April 20

	Room A	Room B	Room C	Room D	Room E
9:00 10:00	**Keynote Lecture IV:** Connected Smart EVs save the World Tsuguo Nobe, Nagoya University Chairs: T. Hatakeyama, Toyama Prefectural Univ., Y. Morikawa, ULVAC				
10:00 10:10	**Break**				
10:10 11:50	**TA1: Kyushu-Kumamoto Session-1** Chairs: M. Aoyagi, Kumamoto Univ., K. Yasuda, Osaka Univ. **TA1-1 <Session Invited>** Research and Development Facilities for Fast Manufacturing IoT Device Prototyping in AIST Kyushu Hisatoshi Hirai, Mitsuru Ozono, Takatoshi Ishikawa, Eishi Maeda, National Institute of Advanced Industrial Science and Technology / Japan **TA1-2 <Session Invited>** The Launch of New Curriculum for Semiconductor Engineer Development at SASEBO KOSEN Yusuke Hibino, Takeshi Ihara, Tamiko Ohshima, Yuki Johno, Hiroshi Nakashima, National Institute of Technology, Sasebo College / Japan **TA1-3** Battery-Less Environmental Sensor Platform for Enclosures in a Zoo Haruichi Kanaya[1], Masafumi Kawano[2], Shun-ichi Shinohara[2], Osamu Takiguchi[3], Hirofumi Nogami[1], [1]Kyushu University, [2]Omuta City Zoo, [3]ALSENS / Japan	**TB1: Advanced Packaging-2** Chairs: Y. Sato, AGC, J. Wang, Meisei Univ. **TB1-1** A New Authentication Method Using The Smart Individuality Printing to Improve The Traceability of Semiconductor Packages Ken Takano[1], Atsushi Miyazaki[2], Mamoru Saito[2], Masaaki Sugimoto[2], Tadatomo Yamada[1], Shinya Takyu[1], [1]LINTEC, [2]Elephantech / Japan **TB1-2** Assembly and Packaging Technology on Silicon-Ceramic-Based Composite Substrates C. Kleinholz, M. Fischer, J. Muller, Technische Universitat Ilmenau / Germany **TB1-3** Thin Die Flip Chip Process Enablement for Stacked IC Memory Packages Chen-Yu Huang[1], Jungbae Lee[1], Tsung-Han Chiang[1], Kohan Lin[1], Chong Leong Gan[1], Travis Jensen[2], [1]Micron Memory Taiwan / Taiwan, [2]Micron Technology / USA **TB1-4** How to Enhance Sn-Bi Low-temperature Solder by Alloying? Shih-kang Lin[1], Chih-han Yang[1], Yu-chen Liu[1], Yuki Hirata[2], Hiroshi Nishikawa[2], [1]National Cheng Kung University / Taiwan, [2]Osaka University / Japan	**TC1: DMR-Mechanical-1** Chairs: H. Sakamoto, Huawei Technologies Japan, R. Miyazawa, IBM Japan **TC1-1** Low Cycle Fatigue of an Interface Between a Substrate and Molding Resin in a Power Module Toru Ikeda[1], Shu Nakagawa[1], Masaaki Koganemaru[1], Takeshi Kakara[2], [1]Kagoshima University, [2]Sumitomo Bakelite / Japan **TC1-2** An Accurate Estimate of Effective Thermal-Mechanical Properties of Coreless Circuit Substrate for Advanced Packaging W. Y. Jhu, H. C. Cheng, Feng Chia University / Taiwan	**TD1: Process-1** Chairs: Y. Morikawa, ULVAC, S. Takyu, LINTEC **TD1-1** Fabrication of Flexible Integrated Circuits with FDSOI on Plastic Substrate for CMOS Image Sensors M. Goto, S. Imura, T. Sakai, H. Sato, NHK Science & Technology Research Laboratories / Japan **TD1-2** Study of High-Speed Bonding Process with Thin Adhesive for Chiplet Heterogenous Integration T. Kudo[1,2], Y. Satake[1,2], T. Funaki[1,2], N. Araki[1,3], Z. Chen[1,4], T. Nakamura[1], T. Ohba[1], [1]Tokyo Institute of Technology, [2]Murata Manufacturing, [3]DAICEL, [4]DISCO / Japan **TD1-3** Robust Measurement of Bonding Strength for Wafer-to-Wafer 3D Integration Junya Fuse, Tomoya Iwata, Sodai Ebiko, Fumihiro Inoue, Yokohama National University / Japan **TD1-4** Laser-assist 3D Selective Structuring on SiP Module AiP Application M. H. Chen, Y. C. Lin, Y. C. Chou, Advanced Semiconductor Engineering / Taiwan	**TE1: LED** Chairs: M. Fujino, AIST, O. Suzuki, Rapidus **TE1-1 <Session Invited>** Properties of Eu(III)-β-Diketonates with Different Phosphine Oxide-Structures and Their Future Applications for LEDs Hiroki Iwanaga, Toshiba / Japan **TE1-2 <Session Invited>** Monolithic Vertically Stacked RGB LEDs for Small Micro-LED Displays with Ultrahigh Definition Yasufumi Fujiwara, Shuhei Ichikawa, Dolf Timmerman, Jun Tatebayashi, Osaka University / Japan **TE1-3 <Session Invited>** Optimum Specification of LED for Strawberry Cultivation in a Closed Space Like a Building Hirohisa Sato, Akinobu Habe, Kyowa / Japan **TE1-4 <Session Invited>** 405nm LED-based White LED Technologyes to Open the New ERA: General Illumination and Inactivation of Virus Atsushi Okuno[1], Jang Uk An[2], [1]Green Planets / Japan, [2]ALLIX / Republic of Korea
11:50 12:40	**Lunch Time**				
12:40 14:20	**TA2: Kyushu-Kumamoto Session-2** Chairs: M. Aoyagi, Kumamoto Univ., T. Ishigure, Keio Univ. **TA2-1 <Session Invited>** Educational Program for Next-Generation Semiconductor Device & Packaging Technology in Kumamoto University Masahiro Aoyagi, Kumamoto University / Japan **TA2-2 <Session Invited>** Possibilities of Semiconductor and Integrated Circuit Design Education for Early Age and Multiple Generations Yohei Ishikawa, National Institute of Technology, Ariake College / Japan **TA2-3 <Session Invited>** Tokyo Electron Kyushu-National Institute of Technology, Kumamoto College of Technology Human Resource Development Program (Practical Activities of Long-Term Internship) Yuji Matsuyama, TOKYO ELECTRON KYUSHU / Japan	**TB2: Advanced Packaging-3** Chairs: N. Fujimori, OLYMPUS, M. Nakazawa, Sony Semiconductor Solutions **TB2-1** High-productivity Patterning for Advanced Package by Combination of the Optical Engine Equipped with Unique Spatial Light Modulator and the Highspeed/Accuracy Stage Control Technology Yuichi Hanada, Minoru Mizubata, Yasumitsu Fujisawa, Takuya Kawashima, SCREEN Holdings / Japan **TB2-2** In-situ Observation of Underfill Dispensing Process Dyi Chung Hu[1], Erh Hao Chen[1], Jeffrey ChangBing Lee[2], Chia Peng Sun[3], Yu En Liang[3], [1]SiPlus, [2]Integrated Service Technology, [3]CoreTech System (Moldex3D) / Taiwan **TB2-3** Double Layer Wiring on Fabric Using Soft Polyurethane Film Substrate and Its Application to Motion Capture Devices Hayato Takahashi, Naoto Tomita, Seiichi Takamatsu, Michitaka Yamamoto, Toshihiro Itoh, The University of Tokyo / Japan	**TC2: DMR-Machanical-2** Chairs: T. Ikeda, Kagoshima Univ., H. Sakamoto, Huawei Technologies Japan **TC2-1** FOPOP Warpage Analysis for Package Design Optimization Ken Zhang, Vito Lin, Teny Shih, Andrew Kang, YuPo Wang, Siliconware Precision Industries / Taiwan **TC2-2** Highly Reliable Laser-sintered Copper FilmsTransformed from Cu_2O Nanoparticles by Plasma Modification of the Polymeric Substrate Surface Wei-Hang Cheng, Wei-Rong Yang, Jenn-Ming Song, National Chung Hsing University / Taiwan **TC2-3** Significant Consumption of Ni-P Layer in Ni-P/Sn-0.7Cu Solder Joints during Thermomigration Satoshi Oya[1,2], Hiroaki Tatsumi[2], Hiroshi Nishikawa[2], [1]Qualtec, [2]Osaka University / Japan **TC2-4** Effect of Bonding Position between Cu Wire and Al Pad in THB Reliability Test Kazutaka Shinohara, Tatsuya Kobayashi, Akira Miyota, Renesas Electronics / Japan	**TD2: Process-2** Chairs: K. Hirano, Panasonic Holdings, Y. Morikawa, ULVAC **TD2-1** Surface Modification of Cyclo Olefin Polymer Film for Electronic Packaging by Vacuum Ultraviolet Irradiation Taro Arimoto, Masaki Miura, Fumitoshi Takemoto, USHIO / Japan **TD2-2** Study of the Behavior of the Functional Group on the Direct Copper Sputtered Interface Using Vacuum Ultraviolet Light S. Endo[1,2], A. Shimizu[1], H. Ueyama[3], K. Fukada[3], Y. Kashiwagi[3], [1]Ushio, [2]Osaka Prefecture University, [3]Shibaura Machine / Japan **TD2-3** Effect of Etching Gas on Adhesion between Mold Resin and Sputtered Stainless Steel Ground Films in Electromagnetic Shield Packages Soichi Homma[1,2], Daichi Okada[1], Akihito Sawanobori[1], Susumu Yamamoto[1], Takashi Imoto[1], Hiroshi Nishikawa[2], [1]Kioxia, [2]Osaka University / Japan **TD2-4** A Study of Underfill Dispensing Patterns in Flip-Chip Packaging Dao-Long Chen[1], Hui-Jing Chang[1], Tang-Yuan Chen[1], Yung-Hsiang Hu[1], Ting-Bin Chen[1], Chi-Hung Pan[1], Yu-Shuo Yang[2], Sheng-Jye Hwang[2], [1]Advanced Semiconductor Engineering, [2]National Cheng Kung University / Taiwan	**TE2: IMPACT Session** Chairs: J. Mizuno, National Cheng Kung Univ., K. N. Chiang, National Tsing Hua Univ. **TE2-1 <Session Invited>** Simulation of Laser-Assisted Bonding Process by the Phase-field Method Tai-Yu Pan, Wen-Dung Hsu, Nation Cheng Kung University / Taiwan **TE2-2 <Session Invited>** Understanding Peculiar Behaviors of Electronic Materials Through Phase Diagrams Sinn-wen Chen, National Tsing Hua University / Taiwan **TE2-3 <Session Invited>** Predicting Void Reduction of Flip Chip Package in the Pressure Oven L.H. Shen[1], C.T. Wu[1], D.C. Hu[2], E.H. Chen[2], Jeffrey C.B. Lee[3], [1]CoreTech System (Moldex3D), [2]SiPlus, [3]iST-Integrated Service Technology / Taiwan **TE2-4 <Session Invited>** Advanced Substrate for Multi-chip Integration Yu-Hua Chen, Unimicron / Taiwan
14:20 14:30	**Break**				
14:30 16:10	**TA3: 3DIC-1** Chairs: T. Ohba, Tokyo Institute of Technology, S. Uegaki, Crane Research **TA3-1 <Session Invited> 50min.** CMP Challenges in the Era of 3DIC Ji Chul Yang, EBARA Technology / USA **TA3-2** A Temporary Bonding De-Bonding Tape with High Thermal Resistance and Excellent TTV for 3DIC Yuji Sakamoto, Ryoichi Watanabe, Izumi Daido, Toshio Takahashi, SEKISUI CHEMICAL / Japan **TA3-3** Copper Contamination Control in Hybrid Copper Bonding Wooyoung Kim, Seung Ho Han, Yongin Lee, Donggap Shin, Wonyoung Choi, Jiwon Moon, Kyeongbin Lim, BumKi Moon, Minwoo Daniel Rhee, Samsung electronics / Republic of Korea	**TB3: Advanced Packaging-4** Chairs: F. Inoue, Yokohama National Univ., J. Wang, Meisei Univ. **TB3-1** High Density RDL Interconnection of Die to Die using Chip-First Process for Heterogeneous Integration (HI) YoungGun Han[1], Taka Kanayama[1], Hisamitsu Mitsutomi[2], Kanta Nogita[2], Tadashi Suetsugu[1], [1]Fukuoka University, [2]Fukuoka IST / Japan **TB3-2** Electroplating Uniformity Enhancement for High Performance Fan-Out Panel Level Packaging Yuan-Feng Chiang, Boyin Wu, Mingtzung Kuo, Jeffrey Yang, Jen-Kuang Fang, Advanced Semiconductor Engineering / Taiwan **TB3-3** Micro Ball Mount Process for High Performance Fan-Out Large Panel Level Packaging Back-end Process Powei Lu, Jia Sang Weng, Huang Han Chen, Jeffrey Yang, Jen-Kuang Fang, Advanced Semiconductor Engineering / Taiwan	**TC3: Power Electronics-1** Chairs: Y. Ikeda, Fuji Electric, Y. Morikawa, ULVAC **TC3-1** Non-destructive and Destructive Evaluation of Cu-Sinter Joints H.J. Albrecht[1], D. Busse[1], A. Dahlbüdding[1], A. Hutzler[2], O. Rämer[3], [1]budatec, [2]Bondpulse, [3]Fraunhofer Institut / Germany **TC3-2** Robust Bonding at 175°C of Pressureless Ag Nanoparticle Sinter Joint on Ni/Au Finished Cu Substrates in Air Seoah Kim[1,2], Min-Su Kim[1], Sungwook Mhin[2], Dongjin Kim[1], [1]Korea Institute of Industrial Technology, [2]Kyonggi University / Republic of Korea **TC3-3** Copper and Silver Sintered Die-Attach Compared in HVv-Hh3TRB and Thermal Shock Cycling Felix Steiner[1], Dai ishikawa[2], Hideo Nakako[2], Thomas Blank[1], [1]Karlsruhe Institute of Technology / Germany, [2]Resonac / Japan **TC3-4** Influence of Interfacial Interaction on the Reliability of the Bond Between Encapsulation Epoxy and Copper Substrate Shuaijie Zhao[1], Chuantong Chen[1], Minoru Ueshima[2], Motoharu Haga[2], Katsuaki Suganuma[1], [1]Osaka University, [2]Daicel / Japan	**TD3: Organic & Polymer Material** Chairs: G. Hamasaka, Tokuyama, T. Onishi, Grand Joint Technology **TD3-1** Fabrication and Evaluation of Microfluidic Organic-Light Emitting Diode Having a Fluorine-Doped Tin Oxide Cathode Ryuto Ikeda[1], Jun Mizuno[2], Takashi Kasahara[1], [1]Hosei University / Japan, [2]National Cheng Kung University / Taiwan **TD3-2** Development of Ultra-Low Chlorine Epoxy Resins for Highly Reliable Electronics Ryo Yoshimura, Wataru Urano, Yuuki Asuma, Kazumasa Ota, Mitsubishi Chemical / Japan **TD3-3** Development of Laminate Materials with Low Df Using Novel Functionalized PPE H. Yamamoto[1], K. Iwase[1], H. Fukuoka[1], S. Otani[1], M. Harada[2], [1]Asahi Kasei, [2]Kansai University / Japan **TD3-4** Liquid Crystal Mesogenic Epoxy Modified Cyanate Ester Resin S. Yanaura, M. Harada, Kansai University / Japan	**TE3: ISMP Session-1** Chairs: H. Nishikawa, Osaka Univ., O. Suzuki, Rapidus **TE3-1 <Session Invited>** Electrodeposition of Invar alloy for FMM Applications Jae Ho Lee, Hongik University / Republic of Korea **TE3-2 <Session Invited>** Nanoscale Copper Roughness Formation and Its Application Bomook Chung, YMT / Republic of Korea **TE3-3 <Session Invited>** Effective Thermal Property Mapping of Semiconductor Packages for Thermal Management Based on Convolution Neural Network Jeong-Hyeon Park[1], Kyung-bin Kim[1], Hwanjoo Park[2], Sunggu Kang[2], Sungho Mun[3], Jaechoon Kim[3], Eun-Ho Lee[1,2], [1]Sungkyunkwan University, [2]Sungkyunkwan University, [3]Samsung Electronics / Republic of Korea **TE3-4 <Session Invited>** Strategies for Mechanically Reliable Thin-Film Flexible Electronics Taek-Soo Kim, KAIST / Republic of Korea
16:10 16:50	**Break / Poster Session**				
16:50 18:30	**TA4: 3DIC-2** Chairs: N. Fujimori, OLYMPUS, T. Nonaka, Rapidus **TA4-1 <Session Invited> 50min.** Die-to-Wafer and Wafer-to-Wafer Hybrid Bonding for Heterogeneous Integration Hiroshi Yamamoto, EV Group Japan / Japan **TA4-2** Physical Properties of Large Cu Grain and Application to Cu-SiO2 Hybrid Bonding R. Kobayashi[1], E. Sone[1], M. Sawa[1], M. Murugesan[2], T. Fukushima[2], [1]JCU, [2]Tohoku University / Japan **TA4-3** Time Evolution Study of Two-Step Plasma-Treated Copper-Copper Direct Bonding in Ambient Liangxing Hu[1], Yu Dian Lim[1], Peng Zhao[1], Michael Joo Zhong Lim[1], Weiyang Miao[1], Van Quy Dinh[1], Xin Ju[2], Chuan Seng Tan[1,2], [1]Nanyang Technological University, [2]A*STAR / Singapore	**TB4: Advanced Packaging-5** Chairs: T. Aoki, IBM Japan, Y. Sato, AGC **TB4-1** Materials Technology Correlation Between Front-end and Back-end Processes in Advanced Semiconductor Industry Kosuke Watahiki[1], Yoshihiro Midoh[2], Kazuya Okamoto[1,2,3], [1]Yamaguchi University, [2]Osaka University, [3]Tokyo Metropolitan University / Japan **TB4-2** A Deep Learning Reconstruction Technique and Workflow to Enhance 3D X-ray Imaging Resolution and Speed for Electronics Package Failure Analysis Allen Gu[1], Andriy Andreyev[1], Masako Terada[1], Thomas Rodgers[2], Vignesh Viswanathan[3], [1]Carl Zeiss Research Microscopy Solutions / USA, [2]Carl Zeiss Microscopy / Germany, [3]Carl Zeiss / Singapore **TB4-3** A Machine Learning Approach to Explore Tensile Properties of Low-Temperature Solders Yu-chen Liu, Ahmad Kholik, Shih-kang Lin, National Cheng Kung University / Taiwan	**TC4: Power Electronics-2** Chairs: M. Aoyagi, Kumamoto Univ., Y. Ikeda, Fuji Electric **TC4-1** Reliability Prediction Platform of SiC Half Bridge Power Module J. Y. Syu, Y. C. Huang, Y. C. Liu, P. K. Chiu, K. S. Kao, T. C. Chang, Industrial Technology Research Institute / Taiwan **TC4-2** Effect of Thermal Cycle Temperature Gap on Thermal Fatigue of Metallized Silicon Nitride Substrates for SiC Power Modules Hiroyuki Miyazaki, Minh Chu Ngo, Kiyoshi Hirao, Manabu Fukushima, National Institute of Advanced Industrial Science and Technology / Japan **TC4-3** Large-Area Ag/Cu Pastes Sintering on Cu Base Plates for Power Module Packaging Chin-Hao Tsai[1,2], Felix Steiner[1], Dai Ishikawa[3], C. Robert Kao[2], Thomas Blank[1], [1]Karlsruhe Institute of Technology / Germany, [2]National Taiwan University / Taiwan, [3]Resonac / Japan **TC4-4** Thermal Impact of Solder Voids under Chip of Power Semiconductors T. Tabakoya, M. Arai, D. Inoue, K. Murakami, K. Matsuo, R. Tsujimura, Toshiba Electronic Devices & Storage / Japan	**TD4: Matal Pastes** Chairs: G. Hamasaka, Tokuyama, K. Hasegawa, JSR **TD4-1** Reliability Evaluation of SiC/Cu Substrate Die-attached Modules with Sintered Cu Joint and Pb-free Solder Ming-chun Hsieh[1], Aiji Suetake[1], Zheng Zhang[1], Rieko Okumura[1], Kei Anai[2], Satoshi Konno[2], Katsuaki Suganuma[1], [1]Osaka University, [2]Mitsui Mining & Smelting (MITSUI KINZOKU) / Japan **TD4-2** Effect of Chemical Factors on Electrical Conductivity of Interconnection Between Carbon-Nanotube-Filled Conductive Pastes and Copper Electrodes Masahiro Inoue, Subaru Tsujimura, Gunma University / Japan	**TE4: ISMP Session-2** Chairs: H. Nishikawa, Osaka Univ., O. Suzuki, Rapidus **TE4-1 <Session Invited>** Microstructure and Mechanical Property of Soldering using Photonic Energy Taejoon Noh, Kyung Deuk Min, Seung-Boo Jung, Sungkyunkwan University / Republic of Korea **TE4-2 <Session Invited>** A Novel Selective EMI Shielding Process by Exploiting Tape Attach and Detach Sub-processes Wonyong Choi[1], David Bokwoo Han[1], Keejun Han[2], [1]Genesem, [2]Hansung University / Republic of Korea **TE4-3 <Session Invited>** Inkjet Printing Technology for Semiconductor Packaging Seog Soon Kim, UniJet / Republic of Korea **TE4-4 <Session Invited>** Advanced Metallizations for Next Generation Semiconductor Packaging Technology Bongyoung Yoo, Hanyang University / Republic of Korea
18:40 19:40	**Sponsors Exhibition Party**				

Friday, April 21

	Room A	Room B	Room C	Room D	Room E
9:00 10:40	**FA1: Pan-pacific Session** Chairs: C. E. Bauer, TechLead, O. Suzuki, Rapidus **FA1-1 <Session Invited>** The New Tech Frontier for Healthcare Matthew Hudes, bdlBiologx / USA **FA1-2 <Session Invited>** Breakthrough Technology to Improve Semiconductor X-Ray Results Keith Bryant, Excillum / Sweden	**FB1: Optoelectronics-1** Chairs: T. Aoki, IBM Japan, Y. Sato, AGC **FB1-1 <Session Invited> 50min.** IOWN Brought by Photonics-Electronics Convergence Devices Yuzo Ishii, NTT / Japan **FB1-2 <Session Invited> 50min.** Nanophotonics Toward On-chip Photonic Integration A. Shinya[1,2], S. Kita[1,2], K. Ikeda[1,2], K. Nozaki[1,2], T. Ishihara[4], S. Matsuo[1,3], M. Notomi[1,2], [1]NTT Nanophotonics Center, [2]NTT Basic Research Laboratories, [3]NTT Device Technology Laboratories, [4]Nagoya University / Japan	**FC1: High-Speed, beyond 5G and mmWave** Chairs: T. Onishi, Grand Joint Technology, K. Yamada, Toshiba **FC1-1** Design of Dual-Band Antenna in Package with Steerable Beam for 5G mmWave Communication Systems Sheng-Chi Hsieh, Hong-Sheng Huang, Wen-Chun Hsiao, Cheng-Yu Ho, Chen-Chao Wang, Advanced Semiconductor Engineering / Taiwan **FC1-2** Effect of Ni Additive on Electroless CU Quality for High Density Interconnect PCB Substrate Zheng Zhang[1], Ming-Chun Hsieh[1], Masahiko Nishijima[1], Aiji Suetake[1], Hiroshi Yoshida[1], Rieko Okumuara[1], Chuantong Chen[1], Hidekazu Homma[2], Koji Kita[2], Katsuaki Suganuma[1], [1]Osaka University, [2]Okuno Chemical Industries / Japan **FC1-3** Fabrication of High-speed Signal Transmission Rigid Substrate by Silver-seed Copper Plating Technique Rei Tamura, Norimasa Fukazawa, Wataru Fujikawa, DIC / Japan **FC1-4** Electroless Plating on Coiled Algae to Copper Microcoils and Their Terahertz Electromagnetic Wave Absorption Keita Arikiyo[1], Tomokazu Iyoda[1,2], Koji Kita[1], Joonhaeng Kang[1], Yukihiro Tanida[3], Naoya Kurahashi[3], Masahiro Koide[4], Toshichika Ooki[4], [1]Okuno Chemical Industries, [2]Doshisha University, [3]Kyoto Prefectural Technology Center for Small and Medium Enterprises, [4]Panac / Japan	**FD1: Thermal Management-1** Chairs: H. Sakamoto, Huawei Technologies Japan, K. Takeuchi, Tohoku Univ. **FD1-1** Fine Fin Structure Suitable for SiC Inverter Cooling with Subcooled Flow Boiling Hitoshi Yoshimura[1], Kazuhisa Yuki[2], Noriyuki Unno[2], Takuro Nakaoka[1], Mutsuaki Goto[1], [1]DENSO, [2]Sanyou-Onoda City University / Japan **FD1-2** Heat Transfer Enhancement in Two-phase Immersion Cooling with FC-72 D. Tanaka[1], K. Yuki[1], N. Unno[1], K. Yuki[1], T. Ide[2], T. Ogushi[2], M. Murakami[2], [1]Sanyo-Onoda City University, [2]Lotus Thermal Solution / Japan **FD1-3** Topology Optimization of a Thermal Conduction Block Using the Thermal Bottleneck Haruki Takei, Siemens / Japan	**FE1: Solder-1** Chairs: K. Hasegawa, JSR, M. Inoue, Gunma Univ. **FE1-1** Development of High Temperature Lead-free Solders in the Al-95Zn + xSn Systems Andromeda Dwi Laksono[1,2], Yee-wen Yen[1], [1]National Taiwan University of Science and Technology / Taiwan, [2]Institut Teknologi Kalimantan / Indonesia **FE1-2** Interfacial Intermetallic Compounds of Bi2Te3/Cu Joint Using SAC305 Solder and Nano-Ag Paste Seongwoo Pak, Hiroaki Tatsumi, Jianhao Wang, Hiroshi Nishikawa, Osaka University / Japan **FE1-3** Electromigration in Tin-Bismuth Planar Solder Joints Prabjit Singh[1], L. Palmer[1], M. Hamid[1], T. Wassick[1], R. F. Aspandiar[2], B. Franco[2], H. Fu[3], Richard Coyle[4], Faramarz Hadian[5], V. Vasudevan[6], A. Allen[7], K. Howell[8], K. Murayama[9], H. Zhang[10], A. Lifton[11], M. Ribas[11], M. Sarangapani[12], T. Munson[13], S. Middleton[13], [1]IBM, [2]Intel / USA, [3]iNEMI / China, [4]Nokia, [5]Physics Dept., [6]Dell Technologies, [7]HP / USA, [8]Nihon Superior, [9]Shinko Electric Industries / Japan, [10]Indium / USA, [11]MacDermid Alpha Electronics Solutions / USA & India, [12]Heraeus Materials Singapore / Singapore, [13]Foresite / USA **FE1-4** Evolution of the Sn-Bi Solder Microstructure vs. Temperature – an In-situ Scanning Electron Microscopy Study Xin F. Tan[1,2], Jiye Zhou[1], Stuart D. McDonald[1], Masahiko Ikeda[3], Kazuhiro Nogita[1], [1]The University of Queensland / Australia, [2]Kyushu University, [3]Nihon Superior / Japan
10:40 10:50			**Break**		
10:50 12:30	**FA2: Chiplet-1** Chairs: Y. Orii, Rapidus, O. Suzuki, Rapidus **FA2-1 <Session Invited> 50min.** Challenges and Opportunities with Chiplets? Where Do We Go Next? Jan Vardaman, TechSearch International / USA **FA2-2 <Session Invited> 50min.** Advanced Packaging Technology Solutions and Hybrid Design Platform for Chiplets Integration Lihong Cao, ASE (US) / USA	**FB2: Optoelectronics-2** Chairs: T. Onishi, Grand Joint Technology, S. Takyu, LINTEC **FB2-1 <Session Invited> 50min.** Current Status and Future Prospects of Optical Interconnection Based on Si Photonics Technology Kazuhiko Kurata, AIO Core / Japan **FB2-2** Quantum Dot Color Conversion Film with Enhanced Color Rendering Performance Yuanjie Cheng, Jeffery C. C. Lo, Xing Qiu, Hua Xu, Mian Tao, S. W. Ricky Lee, Hong Kong University of Science & Technology / Hong Kong **FB2-3** A Novel 3D Structure with 2D Addressable VCSEL Arrays and Laser Diode Driver for Solid-State LiDAR Hirohisa Yasukawa[1], Kiyohisa Sakai[1], Masashi Nakazawa[1], Gyongsok Song[1], Hideki Watanabe[1], Yasutaka Higa[1], Rintaro Koda[1], Yoshio Konishi[2], Hayato Kamizuru[2], Hayato Iwamoto[1], [1]Sony Semiconductor Solutions, [2]Sony Semiconductor Manufacturing / Japan	**FC2: Sensing Device** Chairs: N. Fujimori, OLYMPUS, F. Uchikoba, Nihon Univ. **FC2-1** Strain-Induced Change of Gas Adsorption Properties of Graphene and its Application to a Gas Sensor Xiangyu Qiao, Meng Yin, Ken Suzuki, Hideo Miura, Tohoku University / Japan **FC2-2** Bluetooth Wireless Mouthguard Sensor for Real-time Measurement of Saliva Glucose as Oral Information Kohji Mitsubayashi[1], Gentaro Kawase[1], Kenta Iitani[1], Takahiro Arakawa[2], Dzung Viet Dao[3], [1]Tokyo Medical and Dental University, [2]Tokyo University of Technology / Japan, [3]Griffith University / Australia **FC2-3** Development of a Compact Module for Deep-body Temperature Measurement Shoya Fukui, Nobuaki Hashimoto, Suwa University of Science / Japan **FC2-4** LPWA Based Module for Forest Fire Detection Eunsol Jo, Cheong-Ha Jung, Gu-Sung Kim, Kangnam University / Republic of Korea	**FD2: Thermal Management-2** Chairs: T. Ikeda, Kagoshima Univ. H. Sakamoto, Huawei Technologies Japan **FD2-1** Double-sided <111>-oriented Nanotwinned Copper Foils for Thermal Interface Materials in High Power Electronics Guan-You Shen, Chih Chen, National Yang-Ming Chiao Tung University / Taiwan **FD2-2** Verification Method of the Thermal Interface Resistance by Using Silicon Bare-die Qun Yuan, Wasanthamala Badalawa, Yoshitaka Aoki, SIEMENS / Japan **FD2-3** The Large-area TIM Using Sn-Cu-Ni-Sb Quaternary IMC Joint Material Hiroaki Ikeda, Shigenobu Sekine, Napra / Japan **FD2-4** Pattern Design of SiC-TEG Heater Chip with Uniform Temperature Distribution Applied in Power Module Packaging Fupeng Huo[1], Ye Wang[2], Chuantong Chen[1], Peihao Geng[1], Luobin Zhang[3], Yoshiji Yamaguchi[4], Katsuaki Suganuma[1], [1]Osaka University / Japan, [2]Beihang University / China, [3]Harbin Institute of Technology / China, [4]Yamato Scientific / Japan	**FE2: Solder-2** Chairs: T. Aoki, IBM Japan, G. Hamasaka, Tokuyama **FE2-1** Investigation of the Stability of $CuIn_2$ in Cu-In Phase Diagram F. L. Chang, Y. H. Lin, C. R. Kao, National Taiwan University / Taiwan **FE2-2** Interfacial Reaction Between Silver and Solid Indium I. C. Fang, F. L. Chang, C. C. Chang, C. R. Kao, National Taiwan University / Taiwan **FE2-3** The Influence of Bi Content on Joint Properties Using Sn-Bi-Zn-In Alloy H. Nakawaki[1], H. Tatsumi[1], C. Yang[2], S. Lin[2], H. Nishikawa[1], [1]Osaka University / Japan, [2]National Cheng Kung University / Taiwan **FE2-4** Investigation of Bi and In Elemental Addition in Solder Paste for DRAM Module Reliability Enhancement Yun-Ting Hsu[1], Yung-Sheng Zou[1], Yi-Yu Chen[1], Min-Hua Chung[1], Chong-Leong Gan[1], Fatima Macalalad[1], Shriram Harihara Subramanian[2], [1]Micron Memory Taiwan / Taiwan, [2]Micron Technology / USA
12:30 13:20			**Lunch Time**		
13:20 15:00	**FA3: Chiplet-2** Chairs: Y. Orii, Rapidus, S. Uegaki, Crane Research **FA3-1 <Session Invited> 50mn.** Evolution of BEOL Technology with Scaling Kazuyoshi Ueno, Shibaura Institute of Technology / Japan **FA3-2 <Session Invited>** Overview and Progress of the Chiplet Integration Platform Consortium Meiten Koh[1], Yoichiro Kurita[2], Yasuhiro Morikawa[3], Ichiro Kono[4], Takafumi Fukushima[5], Katsuaki Suganuma[6], [1]Taiyo Ink MFG., [2]Tokyo Insutitute of Technology, [3]ULVAC, [4]AOI Electronics, [5]Tohoku University, [6]Osaka University / Japan **FA3-3 <Session Invited>** Wafer-Level Chiplets Integration Platform Wei-Chung Lo, Industrial Technology Research Institute / Taiwan	**FB3: Ag Sintering Interconnect** Chairs: M. Fujino, AIST, K. Hirano, Panasonic Holdings **FB3-1** Novel Al /AlN Bonding by Micro-Sized Ag Particles Sinter Joining in Low Temperature Low Pressure Air Conditions Chuantong Chen[1], Yang Liu[1], Minoru Ueshima[2], Katsuaki Suganuma[1], [1]Osaka University, [2]Daicel / Japan **FB3-2** Effect of Aging and Thermal Shock on the Reliability of Silver Sintered Die Attach for SiC Power Devices Wangyun Li[1], Chuantong Chen[1], Yang Liu[1], Minoru Ueshima[2], Takeshi Sakamoto[2], Katsuaki Suganuma[1], [1]Osaka University, [2]Daicel / Japan **FB3-3** A Novel and Cost-Effective Ag/Si Composited Paste With Highly Stable Microstructure Maintaince in Thermal Shock Cycles Y. Liu[1], C. Chen[1], M. Ueshima[2], T. Sakamoto[2], T. Naoe1, H. Nishikawa1, K. Suganuma[1], [1]Osaka University, [2]Daicel / Japan **FB3-4** Microstructure and Property of Ag Sintered Joint Doping with Aln Nanoparticles Jianhao Wang, Shogo Yodo, Hiroaki Tatsumi, Hiroshi Nishikawa, Osaka University / Japan	**FC3: Emerging 3D Integration Technologies** Chairs: N. Fujimori, OLYMPUS, S. Takyu, LINTEC **FC3-1** Compensation of the Warpage of CVD Diamond Wafers Using Intermediate Layers for Surface Activated Bonding Junsha Wang, Tadatomo Suga, Meisei University / Japan **FC3-2** Direct Bonding of Germanium and Diamond Substrates by Hydrophilic Bonding Yuki Minowa[1,2], Takashi Matsumae[1], Masanori Hayase[2], Yuichi Kurashima[1], Hideki Takagi[1], [1]National Institute of Advanced Industrial Science and Technology, [2]Tokyo University of Science / Japan **FC3-3** Protection of Activated Au Surface using Self-assembled Monolayer for Room Temperature Bonding Kai Takeuchi[1], Junsha Wang[2], Tadatomo Suga[2], Beomjoon Kim[3], Eiji Higurashi[1], [1]Tohoku University, [2]Meisei University, [3]the University of Tokyo / Japan **FC3-4** Effect of Tafel Slope on the Difference Deposition Rate at 2CD (Circle Diameter) Wafer A. Akita, D. Hashimoto, M. Kiso, S. Hashimoto, C. Uyemura / Japan	**FD3: Thermal Management-3** Chairs: T. Ohba, Tokyo Institute of Technology, H. Sakamoto, Huawei Technologies Japan **FD3-1** Issues of Using Unsaturated Heating Time for Transient Thermal Measurement Tomoaki Hara[1], Shuhei Fukunaga[2], Tsuyoshi Funaki[2], [1]Siemens, [2]Osaka University / Japan **FD3-2** Evaluation of Thermal Resistance Reduction by Thinning Substrate of β-Ga_2O_3 SBD Shota Seki[1], Tsuyoshi Funaki[1], Jun Arima[2], Minoru Fujita[2], Jun Hirabayashi[2], Kazuyoshi Hanabusa[2], [1]Osaka University, [2]TDK / Japan **FD3-3** Investigation Regarding Temperature Prediction Accuracy of Discrete Power Semiconductor Package Models Koji Nishi, Ashikaga University / Japan	**FE3: Solder-3** Chairs: T. Aoki, IBM Japan, O. Suzuki, Rapidus **FE3-1** Hybrid SnBi/SAC Low-Temperature Solder Bump Albert T. Wu[1], Jui-Lin Chao[1], Yu-Yuan Lai[1], Chang-Meng Wang[2], [1]National Central University, [2]Shenmao Technology / Taiwan **FE3-2** The Effects of Solution Treatment and Room Temperature Ageing on Mechanical Properties of Sn-37wt%Bi and Sn-57wt%Bi Xiaozhou Ye[1], Lei Tao[1], Stuart D. McDonald[1], Xin Fu Tan[1], Keith Sweatman[2], Kazuhiro Nogita[1], [1]The University of Queensland / Australia, [2]Nihon Superior / Japan **FE3-3** Impact Strength of Sn58Bi and Sn45Bi2.6Zn0.5In Solder Joints After Isothermal Aging Zhi Jin[1], Shunsuke Fujiwara[2], Junichi Takenaka[2], Koichi Hagio[2], Hiroshi Nishikawa[1], [1]Osaka University, [2]Nihon Genma MFG. / Japan
15:00 15:20			**Break**		
15:20 17:00	**FA4: Chiplet-3** Chairs: Y. Orii, Rapidus, Y. Sato, AGC **FA4-1 <Session Invited>** Chiplet Technologies for HPC and AI Dale McHerron, IBM / USA **FA4-2 <Session Invited>** The Emergence of Chiplet Interconnect Technology: Breaking Boundaries Between FEOL and BEOL Fumihiro Inoue, Yokohama National University / Japan **FA4-3 <Session Invited> 50min.** 3D Super Chip Concept to Build a New Era of Chiplet and Heterogeneous Integration Takafumi Fukushima, Tohoku University / Japan	**FB4: Cu Interconnect** Chairs: M. Fujino, AIST, F. Inoue, Yokohama National Univ. **FB4-1 <Session Invited>** TGV Cu Metallization on Glass Technology Trend Tetsuya Onishi, Grand Joint Technology / Hong Kong **FB4-2** Enhanced Reactivity of Electroless Cu Interconnection by Surface Oxidation Pretreatment Y. C. Lin[1], C. H. Shen[1], C. Y. Hung[1], P. S. Shih[1], J. H. Huang[1], C. L. Kao[2], Y. S. Lin[2], Y. C. Hung[2], C. R. Kao[1], [1]National Taiwan University, [2]Advanced Semiconductor Engineering Group / Taiwan **FB4-3** Molecular Dynamics Simulation of Cu-Cu Solid-State Bonding under Various Bonding Parameters Hiroaki Tatsumi[1], C.R. Kao[2], Hiroshi Nishikawa[1], [1]Osaka University / Japan, [2]National Taiwan University / Taiwan **FB4-4** Study of Cu Micro-via by TOF-SIMS and STEM Masahiko Nishijima[1], Ming-Chun Hsieh[1], Zhang Zheng[1], Aiji Suetake[1], Hiroshi Yoshida[1], Rieko Okumuara[1], Chuantong Chen[1], Hidekazu Homma[2], Koji Kita[2], Katsuaki Suganuma[1], [1]Osaka University, [2]Okuno Chemical Industries / Japan			**FE4: Advanced Package Material** Chairs: G. Hamasaka, Tokuyama, K. Hasegawa, JSR **FE4-1** Novel Photo Imageable Film for Interlayer Insulation Application Meiten Koh, Kazuyoshi Yoneda, Nakada Kazutaka, Yuna Kawata, Kensuke Naka, Taiyo Ink MFG. / Japan **FE4-2** 1/1 μm Line and Space Cu Wiring with Organic Dielectric Through High Electrical Reliability Yu Shoji, Takuma Nishimura, Hisashi Ogasawara, Keika Hashimoto, Yuki Masuda, Hitoshi Araki, Masao Tomikawa, Toray Industries / Japan **FE4-3** Novel Temporary Bonding/Debonding System Enabling Advanced Packaging Process Emi Miyazawa, Tetsuya Enomoto, Yuta Akasu, Shogo Sobue, Yuki Nakamura, Saeko Ogawa, Takashi Kawamori, Resonac / Japan **FE4-4** Liquid Compression Mold Underfill Designed for One-Step Encapsulation in Overmold Process Yuto Shigeno, Yukihiro Ikeda, Kyota Aoyama, Tsuyoshi Kamimura, NAMICS / Japan