April 18 (Wed.)

9:50

OPENING CEREMONY

10:00

WA1: 3D Packaging

Chairperson:R. Tummala (Georgia Institute of Technology)
H. Nishida (IBM Japan)

1. **Stacked Semiconductor Packages (Invited)**
   S. Denda, T. Otake, Y. Tezuka, Nagano Institute of Technology / Japan
2. Micro Bump Interconnections and Encapsulation Technologies on 3D Stacked LSI
   Y. Tomita, T. Morifuji, T. Ando, M. Tago, R. Kajiwara, Y. Nemoto, T. Fujii, T. Sato, K. Takahashi,
   Association of Super-Advanced Electronics Technologies (ASET) / Japan
3. Development of 3D-module
   K. Sato, Shindo / Japan
4. Development of Stackable 0.5mm Thickness FBGA Package
   M. Chino, K. Tsuchihashi, K. Miyajima*, Misuzu Industries, *Toshiba / Japan
5. 128Mbit NAND Flash Memory by Chip on Chip Technology with Cu Through Plug
   K. Sasaki, M. Matsuo, N. Hayasaka, K. Okumura, Toshiba / Japan
6. Stacked Extremely Thin Chip Scale Package
   A. Yoshida, Amkor Technology / U.S.A.
7. High-density Interconnection 3D Packaging Module for CCD Micro-camera System
   H. Yamada, T. Togasaki, H. Sudo, Toshiba / Japan

WB1: Pb-free Solders

Chairperson:C. Bauer (TechLead)
K. Matsubara (Sharp)

1. Environmentally Preferred Packaging: Pb-free Solders
   D. Frear, Motorola / U.S.A.
2. Effect of Additional Elements on Wettability for Pb-free Solder of Sn-3.0Ag-0.5Cu
   M. Miyazaki, Oki Electric Industry / Japan
3. Microstructures of Sn-Ag-Cu Solders Solidified with Various Cooling Rates
   T. Narita, Hokkaido University / Japan
4. Characteristics of Sn-Ag-Cu Solder and Interfaical Reaction between Lead-free Metallization and Solder
   M. Kitajima, M. Takesue, T. Shono, K. Yamazaki*, M. Noguchu*, Fujitsu, *Fujitsu Laboratories / Japan
5. Evaluation on the Properties of Sn-Ag-Bi Solder with Low Melting Point
   H. Shimokawa, Hitachi / Japan
6. Interface Microstructures of Sn-Zn-Bi Solder Metal Plating and Their High Temperature Stability
   Y.-S. Kim, Osaka University / Japan
7. Metallurgical Reaction between Electroless Ni Metallized Al_2O_3 Substrate and Unleaded 42Sn-58Bi Solders during Annealing
   J.-G. Duh, National Tsing Hua University / Taiwan

12:55

LUNCH TIME

13:50

Messages to the 21st Century

Chairperson:F. Miyashiro (IME)

15:00

Invited Speeches

Chairperson:K. Hashimoto (Fujitsu Laboratories)

1. **SOP vs. SOC**
   Prof. Rao R. Tummala, Georgia Institute of Technology / U.S.A.
2. **Optical Hybrid Integrated Circuit**
   Dr. Yasufumi Yamada, NTT Electronics / Japan

16:40

AWARDING CEREMONY

16:55

17:45

WELCOME RECEPTION

Sky Hall “Fontaine”
World Trade Center Bldg. 38F.

19:45