April 18 (Thu.)

9:30

TA1: Advanced Packaging

Chairperson: C. E. Bauer (TechLead)
M. Tsukamoto (Matsushita Electric Industrial)

1. **Recent Advances in Integral Passives Research at Georgia Tech (Session Invite)**
   R. R. Tummala, S. Bhattacharya, S. Dalmia, P. M. Raj, T. Ogawa, S. H. Lee, R. Mani, A. Bavisi, F. Ayazi, Georgia Institute of Technology / U.S.A.
2. **The Growth of the Flip Chip Market: New Applications and Developments (Session Invite)**
   E. J. Vardaman, TechSearch International / U.S.A.
3. Digital, RF and Optical Integration in System-on-a-Package (SOP)
   V. Sundaram, F. Liu, S. Dalmia, J. Hobbs, E. Matoglu, M. Davis, Georgia Institute of Technology / U.S.A., T. Nonaka, M. Swaminathan, N.-M. Jokerst, Toray Limited, Japan / Japan
4. Fine Pitch Wire Bond Dual Damascene Copper Chip PBGA Assembly and Its Reliability Performance
   V. Kripesh, M. Sivakumar, S. Srinivasamurthy, R. Rajoo, Institute of Microelectronics, L. A. Lim, ASM Technology Singapore, M. K. Iyer, Institute of Microelectronics / Singapore
5. Embedded Capacitor Formed on PWB for Next Generation Package
   Y. Horikawa, A. Rokugawa, T. Iijima, Shinko Electric Industries / Japan
6. Development of a Low Cost High Performance WB-CSP Package for Wireless Application
   T. C. Chai, V. Kripesh, Y. K. Yeo, D. Pinjala, X. W. Zhang, M. K. Iyer, Institute of Microelectronics / Singapore

11:50

7. Radio-ray Area Detector Using Multi-layer Thin Film Substrate
   T. Motomura, H. Hirai, O. Shimada, Y. Fukuoka, D. T. Cirsuit Technology, T. Tanimori, Kyoto University / Japan

TB1: Plating

Chairperson: E. Zakel (Pac Tech)
A. Okuno (Sanyu Rec)

1. Influence of Impurities in Electroless Ni-P Films
   K. Sugiura, Fukuryo Semicon Engineering / Japan
2. Selective Activating Process for Fine Pattern Deposition
   T. Nishiwaki, Kanto Gakuin University / Japan
3. Cyanide-free Electroless Gold Plating Solution Using Thio-compound as Complexing Agent and Reducing Agent
   D.-H. Kim, Daiwa Fine Chemicals / Japan
4. Electroless Platinum Plating for Electronics Industry
   Y. Ohtani, K. Kitada, Tanaka Kikinzoku Kogyo, R. Toda, Y. Sato, Kanagawa University / Japan
5. Via-Filling and Electrochemical Studies of Additives for Copper Deposition
   S. Miura, Kanto Gakuin University / Japan
6. Sn-Ag Alloy Solder Bump Formation for Flip-chip Bonding Using Electroplating Method
   S. Arai, Shinshu University / Japan
7. Solderability Property of Electroless Gold Plating on the Cu Substrate
   M. Iwasaki, Okuno Chemical Industries / Japan

LUNCH TIME

12:50

TA2: Optoelectronics

Chairperson: S.-K. Chiang (Prismark Partners)
Y. Ando (Fujikura)

1. Demand for Specialist Materials and Components in Optoelectronic Communications Modules
   M. Wuthenow, Prismark Partners / U.S.A.
2. Optical WDM Packet-by-packet Interconnection Modules for 5-Tb/s Electro-optical Switching System
   N. Matsuura, K. Yamakoshi, T. Ohyama, Y. Akahori, E. Oki, N. Yamanaka, NTT / Japan
3. A Photonic Backplane for Reconfigurable Optical Interconnection
   S. Koike, Y. Arai, NTT / Japan
4. Micro-mirror Molding Technology for Opto-electronic Hybrid Modules
   M. Oda, NEC / Japan
5. Optical Packaging Module with Tape-platform Technology
   A. Murata, Seiko Epson / Japan
6. A Modified Flip Chip Bonding Process for VCSEL Array Used for Optical Interconnect
   K.-M. Chu, Korea Advanced Institute of Science and Technology, H.-H. Park, W.-H. Kim, Information and Communications University, D. Y. Jeon, Korea Advanced Institute of Science and Technology / Korea

15:10

7. Design of the Smart Optoelectoronic Exclusive or Gate Based on Multimode Interference Structure
   W.-C. Chang, Tamkang University / Taiwan

TB2: Materials

Chairperson: Z. Kachwalla (CSIRO)
I. Kaneko (Musashi Institute of Technology)

1. Flow Time Measurements for Underfills in Flip-chip Packaging
   J. Wang, Intel Corporation / U.S.A.
2. Novel Underfill Film for Wafer Level Processing
   A. Matsumura, S. Misumi, Y. Hotta, Nitto Denko / Japan
3. Development of the Novel Thermosetting Flux for Flip Chip Assembly
   K. Nagatomi, Y. Sakamoto, S. Katsurayama, Sumitomo Bakelite / Japan
4. Development of Braille Printer Using a Hot-melt Recording Material
   M. Denda, T. Otaka, T. Hoshino, T. Chiba, Nagano Prefectural Institute of Technology, Y. Yonezawa, Shinshu University, S. Denda, Nagano Prefectural Institute of Technology / Japan
5. The Conduction Mechanism of RuO_2/CB System Thick Film Resistors
   A. Zaki, I. Kaneko, Musashi Institute of Technology / Japan
6. Carbon Nitride Thin Films Prepared by Hot-wire Chemical Vapor Deposition for Electronics Device
   M. Aono, S. Aizawa, D. Sakasegawa, N. Kitazawa, Y. Watanabe, National Defence Academy / Japan
7. Evaluation on Properties of Skeleton-structured Ceramic/Aluminum Composites for Heat-sink
   M. Nakata, Osaka University / Japan

COFFEE BREAK

15:30

TA3: Interconnection I

Chairperson: J. Maattanen (Elcoteq Network)
H. Matsubara (Sharp)

1. **High Speed Laser Solder Jetting Technology for Optoelectronics and MEMS Packaging (Session Invite)**
   E. Zakel, L. Titerle, T. Oppert, R. Blankenhorn, Pac Tech / Germany, U.S.A.
2. ACF Bonding Parameter Analysis by Using Dynamic Thermal Reaction and Hydrodynamics Simulation Model
   K. Skurai, IBM Japan / Japan
3. Formulation and Electrical and Mechanical Properties of Anisotropic Conductive Adhesive Pastes
   L. Cao, S. Li, J. Liu, Chalmers University of Technology / Sweden
4. Numerical Analysis of Delamination Failure and Interfacial Adhesion Measurements in Flip Chip Package
   M.-L. Sham, Z. Xu, J.-K. Kim, Hong Kong University of Science & Technology / Hong Kong
5. Direct Mount or Interposer -Mounting Method of Bare SAW Filter onto Antenna Switch Module-
   F. Uchikoba, T. Goi, T. Adachi, B. Moriya, S. Hayashi, F. Kurosawa, S. Tajima, TDK / Japan
6. Study on Chip Mounting Technology for Plastic Film Liquid Crystal Displays(LCDs)
   K. Terashima, Citizen Watch / Japan

17:30

TB3: Simulation

Chairperson: H. Nishida (IBM Japan)
E. Takagi (Toshiba)

1. **Study of Beyond GHz Signal Integrity Under TEM Wave Mode Analysis in Multi-channel Transmission Lines (Session Invite)**
   K. Otsuka, C. Ueda, Meisei University, Y. Odate, T. Usami, University of Tokyo, / Japan
2. Conceptual Simulator for Thermal Design of High Speed and High Density Electronics System
   Y. Iwata, Osaka University / Japan
3. Transmission Performance Interconnections Design by FDTD
   Y. Odate, T. Usami, University of Tokyo, K. Otsuka, Meisei University, T. Suga, University of Tokyo / Japan
4. Analysis of Common Mode Radiation from Ground Planes by Simulation Using Moment and FDTD Method
   H. Kikuchi, Association of Super-Advanced Electronics Technologies / Japan
5. Common-mode Current Due to a Trace on a PCB with a Guard-band -Experiment and FDTD Modeling-
   Y. Kayano, M. Tanaka, Akita University, J. L. Drewniak, University of Missouri-Rolla, H. Inoue, Akita University / Japan