April 19 (Fri.)

9:30

FA1: 3D Pakaging

Chairperson: M.-K. Iyer (Institute of microelectronics)
S. Uegaki (Kyocera)

1. High Aspect Ratio Copper Via Fill Used for Three Dimensional Chip Stacking
   K. Kondo, T. Okamura, J. J. Sun, Okayama University,
   M. Tomisaka, H. Yonemura, M. Hoshino, K. Takahashi, Association of Super-Advanced Electronic Technologies / Japan
2. Superfine Flip Chip Interconnections in 20micromillim-pitch
   T. Morifuji, Y. Tomita, T. Ando, R. Kajiwara, N. Tanaka, T. Sato,
   K. Takahashi, Association of Super-Advanced Electronics Technologies / Japan
3. Reliability Improvement of 4-stacked FBGA Package
   M. Chino, Misuzu Industries / Japan
4. High Reliability Insulation Layer Between Each IC for Stacked IC
   A. Okuno, K. Nakahira, Sanyu Rec / Japan
5. 3D Interconnects at Wafer Level by Wafer Bonding
   V. Dragoi, P. Lindner, T. Glinsner, EV Group, F. Shiraki, EV Group Japan,
   C. Schaefer, EV Group / Austria
6. Encapsulation of 3D Stacked Packages
   H. Quinones, A. Babiarz, L. Fang, Asymtek / U.S.A.
7. Multi Layer Semiconductor Package of Tape-BGA
   I. Kato, Toppan Printing / Japan

11:50

FB1: Interconnection II

Chairperson: Y.-B. Sun (Kyonggi University)
I. Watanabe (Hitachi Chemical)

1. **New Concepts in Flipchip Bump Technology (Session Invite)**
   S. Denda, Nagano Prefectural Institute of Technology / Japan
2. High Density Flip Chip on Flex (FCOF): Process, Materials and Reliability
   J. Maattanen, P. Palm, Elcoteq Network / Finland
3. Development of a Flip-chip Flex BGA Package for High Performance Applications
   P.-S. Teo, Y.-K. Yeo, D. Pinjala, O. N. Khan, X.-W. Zhang, S. Sampath, T.-C. Chai,
   Institute of Microelectronics / Singapore
4. Dynamic Strain Generated Under a Plated Bump During Ultrasonic Flip-Chip Bonding
   N. Watanabe, T. Asano, Kyushu Institute of Technology / Japan
5. Bond Strength Analysis of a In-Au Eutectic Bond Under Various Bonding Conditions
   Z. Kachwalla, R. Chai, CSIRO / Australia
6. Solderability and Thermal Analysis of Solder Bump Material
   Y. F. Liu, F. Liu, K. C. Yang, Y. P. Wang, T. D. Her,
   Siliconware Precision Industries / Taiwan
7. Bouncing of Molten Solder Droplets During Solder Bump Formation
   W. Hsiao, J.-H. Chun, H.-Y. Kim, Massachusetts Institute of Technology / U.S.A.

LUNCH TIME

12:50

FA2: Design and Testing

Chairperson: S.-L. Fu (I-Shou University)
S. Oka (Mitsubishi Electric)

1. Development of Probing Technology for 20micromilli-Pitch Bumps
   M. Tanioka, M. Sunohara, K. Takahashi, Association of Super-Advanced Electronics Technologies / Japan
2. Techniques and Tools for Product-specific Analysis Templates: Towards Enhanced CAD-CAE Interoperability for Simulation-based Design and Related Topics
   R. S. Peak, Georgia Institute of Technology / U.S.A.
3. Power-off Vectorless Test Method for Pin Opens in CMOS Logic Circuits
   M. Hashizume, University of Tokushima / Japan
4. Micro-contact Probe Fabricated Using LIGA Process
   T. Haga, Sumitomo Electric Industries / Japan
5. The New Film Intelligent Electronic Converts Using High Technology Materials for Low Power Discharge Lamps
   T. Sobczyk, J. J. Gondek, S. Kordowiak, W. Mysinski, Technical University of Cracow, B. Kawa, J. Kocol, Technical School of Communications,
   P. Szatynski, Cracow Electronics Works / Poland

14:30

FB2: Thermal Management

Chairperson: C. Zardini (Universite Bordeaux I)
S. Kitajo (NEC)

1. Thermal Interface Material Selection Methodology for High Power Dissipating Multi Chip Package
   D. Pinjala, O. K. Navas, R. Ranjan, S. Srinivasamurthy,
   Institute of Microelectronics / Singapore
2. 3D Thermo -electric Cooler Analysis for Laser Diode Module
   Y. Watanabe, Sumitomo Electric Industries /Japan
3. A Novel Composite Material for Electronic Packaging and Thermal Management - High Reinforcement Content Aluminum Matrix Composites
   G. Wu, Q. Zhang, G. Chen, L. Jian, B. Luan, Harbin Institute of Technology / China
4. Novel Thermal Interface Material Using Complex Metal and Polymer
   I. Suehiro, N. Harada, Y. Hotta, Nitto Denko / Japan

COFFEE BREAK

14:50

FA3: Substrates

Chairperson: H. Quinones (Asymtek)
H. Hozoji (Hitachi)

1. Effects of Power-ground Plane Structure on Radiated Emission from PCB
   S. Haga, Association of Super-Advanced Electronics Technologies / Japan
2. Package Contracted with Fine Pitch IVH for High Pin Count Chip Attachment
   S. Koyama, T. Koyama, N. Katagiri, S. Wakabayashi, Shinko Electric Industries / Japan
3. Simultaneous Formation of Wiring and Via Using Photoinduced Selective Plating
   T. Hiraoka, Y. Hotta, K. Asakawa, S. Matake, Toshiba / Japan
4. Cutting Edge Technologies for Micromachining
   Y. Osako, Electro Scientific Industries / U.S.A.
5. Material Properties of Liquid Crystal Polymer Film and Its Applications in High Density Interconnections
   S. Fukutake, Japan Gore-Tex / Japan
6. Moisture Characteristics and Performance of Halogen-free Laminates
   R. Rajoo, E. H. Wong, Institute of Microelectronic / Singapore

16:50

FB3: Reliability

Chairperson: F. Uchikoba (TDK)
T. Kobayashi (Tohoku Epson)

1. Board Level Reliability Enhancement for the Transfer Molded Wafer Level CSP Packages
   X. Zhang, E. H. Wong, M. K. Iyer, T. B. Lim, Institute of Microelectronics / Singapore
2. Board Level Solder Joint Reliability Modeling of TFBGA Package
   T. Y. Tee, H. S. Ng, K. Sivakumar, STMicroelectronics / Singapore
3. Solder Ball Joint Reliability of Electroless Ni-P/Pd/Au Finish
   T. Noudou, Hitachi Chemical / Japan
4. Study of Polymers and Solder Joint Structures for Wafer Level Packaging Applications
   H. Han, S. C. Choi, Y. S. Ryu, I. H. Chi, K. S. Hwang, Microscale / Korea
5. Observation of Wearout Type C4 Microcrack During Temperature Cycling, and a Accerellation Model Using Finite Element Analysis
   K. Umemoto, A. Yoshimura, A. Gohda, IBM Japan / Japan
6. Reliability of CrCuNi Underbump Metallization
   K. C. Chan, C. P. Cheong, MicroFab Technology / Singapore