Room A

09:00 **[15A-1] Advanced Packaging Ⅰ**

1. A Reliability Test on PBGA Packaging Through Piezoresistive Stress Sensor
   C.H.Liu[1], H.Chung[1], D.W.Yang[1], K.F.Tseng[2], B.J.Lwo[1] ([1]National Defense University, [2]Chin-Min Institute of Technology)/Taiwan
2. Evaluation of the Effect of Packaging Process Parameters on Semiconductor Devices with Low-k Conductive Layers
   T. Yamada[1], M.Masumoto[2], O.Horiuchi[1], H.Tomokage[2] ([1]Fukuoka Industry, Science & Technology Foundation, [2]Fukuoka University)/Japan
3. The Solder Blister Control for Lead Frame Packages
   J.W.Chen[1], S.Lee[1], B.Appelt[2], A.Tseng[2] ([1]Advanced Semiconductor Enginrrring, [2]ASE(US))/Taiwan, USA
4. First Generation of Stretchable No-Light Emitting Display Based on Stretchable Electronic Technologies for Textile Application
   A.Fabrice (IMEC)/Belgium

10:40

10:50 **[15A-2] Advanced Packaging Ⅱ**

1. Low-Temperature Wafer Bonding by Ar-Beam Surface Activation
   Y.-H.Wang, S.Taniyama, T.Suga (The University of Tokyo)/Japan
2. Wafer-to-Wafer Alignment Using Moire Pattern and its Interests for 3D Integration
   C.Wang, T.Suga (The University of Tokyo) /Japan
3. A Multilayer Process for 3D-Molded-Interconnect-Devices to Enable the Assembly of Area Array Based Package Types
   T.Leneke (Otto-von-Guericke University of Magdeburg)/Germany
4. 3D Packaging: up to 30 GHz for Integrated Antenna Front-Ends
   C.Drevon[1], B.Bonnet[1], P.Monfraix[1], R.Chiniard[1], C.Val[2], H.Legay[1], P.Couderc[2], J.-L.Cazaux[1] ([1]Thales Alenia Space, [2]3DPlus) /France

12:30

12:30 13:30 **Lunch time Poster Session**

13:30 **[15A-3] 3D/TSV Ⅰ**

1. Integration of Compliant Bump with Through-Si-Via Technology and Its Application Back-Side Illuminated CMOS Image Sensor(Session Invite)
   T.Asano[1], N.Watanabe[2], I.Tsunoda[2], Y.Takao[1], K.Tanaka[3], T.Higashimachi[4], Y.Yamaji[5], M.Aoyagi[5], T.Kyotani[6], H.Arao[7], Y.Kimiya[8], K.Fukunaga[8], A.Ikeda[1], Y.Kuroki[1], T.Tsurushima[1] ([1]Kyushu University, [2]Fukuoka Industry Science & Technology Foundation, [3]Kyushu Sangyo University, [4]Sojo University, [5]AIST, [6]PMT, [7]JGC Catalysts and Chemicals, [8]Yoshidama Surface Finishing) /Japan
2. 3D Packaging and Interconnect Technologies at CEA-Leti Minatec (Session Invite)
   M.Scannell (CEA-Leti)/France
3. TSV and Wafer Level Packaging Approaches to 3D Packaging
   E.J.Vardaman (TechSearch International)/USA
4. Thermal Characterization of a Three-dimensional (3D) Chip Stack
   K.Matsumoto, Y.Taira (IBM)/Japan
5. Bonding Strength Estimation of BCB Dielectric Film in 3D Stacked IC Packages
   M.-C.Hsieh, C.-Y. Cheng, W.Lee, R.-M. Tain (Industrial Technology Research Institute) /Taiwan

15:35

15:45 **[15A-4] 3D/TSV Ⅱ**

1. Inter Chip Fill for 3D Chip Stack
   A.Horibe, F.amada, J.Knickerbocker, C.Feger (IBM)/Japan
2. Die-cracking Evaluation of Silicon Chip Coverd with Polymer Film for 3D Chip Stacking Packages
   C.-J.Wu[1], M.C.Hsieh[2], K.N.Chiang[1] ([1]National Tsing-Hua Univercity, [2]Industrial Technology Research Institute)/Taiwan
3. Characterisation of Through Silicon Via (TSV) Processes Utilising Mass Metrology
   L.Cunnane, A.Kiermasz, G.Ditmer (Metryx) /UK

17:00

17:10 **[15A-5] 3D/TSV Ⅲ**

1. Cost Effective PVD Solution which Enable TSV Integration in the Emerging 3-D Market
   B.Ninan, A.Wang (Tango Systems)/UK
2. Delivering High Reliability from a Wafer-Scale, Chip-Sized Package Incorporating a Through Silicon Via Solution
   M.Kriman (Tessera)/Israel
3. Development of Interconnect Technology in 25 Micron Pitch for Low Cost CoC(Chip on Chip)
   T.Norimatsu (Fujitsu Microelectronics)/Japan
   (18:25)

18:50

Room B1

[15B1-1] Embedded Substrate Ⅲ

1. Novel Approach in Design and Test of Embedded Capacitors in Organic-based Substrate for Highly Compact RF Systems-in-Package Devices
   C.Romero, J.Lim, Y.H.Yoon, T.Kim, S.Yi (Samsung Electro Mechanics)/Korea
2. Electrodeposition of High-k Titania Thin Films for Embedded Capacitors
   B.K.Roy, J.Cho (State University of New York Binghamton)/USA
3. The Nanotransfer Technology of the PZT Capacitor for the Application of Embedded Substrate
   S.Makino, M.Ichiki, R.Maeda, T.Suga (The University of Tokyo, AIST, JST-CREST)/Japan

(10:15)

(10:25)

[15B1-2] LED

1. Refraction Index, Transmittance and Shape Dependence of Light Extraction from Near-ultraviolet Light-emitting Diode
   H.Hayashi (Yamaguchi University)/Japan
2. Luminous and Thermal Characteristics of High Power Near-ultraviolet LED Packages with Various Chip Arrangemants
   K.Kamon (Yamaguchi University)/Japan
3. Analysis of Thermal Performance for High Power Light Emitting Diodes Lighting Modulus
   W.-H.Chi, T.-L.Chou, C.-N.Han, S.-Y.Yang, K.N.Chiang (National Tsing Hua University) /Taiwan
4. Thick Film Pastes for the Manufacture of Low Cost, Insulated Aluminum Substrates for Use as Integrated Heat Sinks for High Intensity LEDs
   K.Takarabe (ESL Nippon)/Japan
5. The Behavior of Thermal and UV Degradiation between LED Encapsulation and their Devices
   C.-W.Hsu, C.-H.Lin, H.-T.Li, S.-C.Huang, K.-C.Chen (Industrial Technology Research Institute)/Taiwan

12:30 13:30 **Lunch time Poster Session**

13:30 **[15B1-3] Printed Electronics Ⅰ**

1. Printable Electronics on Flexible Substrate by Inkjet Technology (Session Invite)
   S.Nishi (Konicaminolta IJ Technologies)/Japan
2. Palm Top Sized Super Fine Inkjet System and Mask Less Direct Patterning (Session Invite)
   K.Murata, K.Shimizu (Advanced Industrial Science and Technology)/Japan
3. Electric Conductive Film Formations by Ink-jet using Individually Dispersed Nanoparticle Ink formed by Gas Evaporation Method (Session Invite)
   M.Oda (ULVAC)/Japan
4. Inkjet Printing of Silver Nanopaste for Printed Electronics (Session Invite)
   S.Abe (Harima Chemicals)/Japan
5. Silver and Copper Nanoparticles and Their Application to Wring Formation and Joining (Session Invite)
   M.Nakamoto (Osaka Municipal Technical Research Institute)/Japan

15:35

15:45 **[15B1-4] Printed Electronics Ⅱ**

1. Advantages of Ink-Jet Printing in LTCC Production Technology (Session Invite)
   Y.Kawamura (KOA)/Japan
2. Embedded Passives with High Precision and Wide Range Build on Plastic Substrates
   M.Nakayama (NY Industries)/Japan
3. Advanced Fine Line Thick Film Conductors with High Conductivity and Solderability Build by Screen-printing
   D.K. Numakura (DKN Research)/USA

17:00

17:10 **[15B1-5] Printed Electronics Ⅲ**

1. Fabrication of RF Circuit Structures on a PCB Material by Inkjet Printing and Electroless Plating
   A.Sridhar[1], M.Perik[2], J.Reiding[2] ([1]University of Twente, [2]Saxion Hogeschool)/The Netherlands
2. Effects of Cold Crystallization on Morphology and Thermal Charctterstic of Poly (9, 9-di-n-octyl-2, 7-fluorene)(PFO)
   B.-Y.Su[1], H.C.Chen[1], C.L.Chung[1], S.L.Fu[1], C.-Y.Ou[2] ([1]I-Shou University, [2]Research Alliance Taiwan TFT LCD Assciation)/Taiwan
3. Pattering of ITO Microwire Using Laser-induced Thermal Printing Method
   S.Iwasaki[1], T.Sano[1], S.Katsura[2], K.Yoshida[3], A.Nakayama[4], A.Hirose[1] ([1]Osaka University, [2]Nippon Denki Kagaku, [3]General Technology, [4]Ion Technology Center)/Japan
   (18:25)

18:50

Room B2

[15B2-1] Interconnections Ⅰ

1. Effect of the Formation of the Intermetallic Compounds between a Tin Bump and an Electroplated Copper Thin Film on Both Mechanical and Electrical Properties of the Jointed Structures
   S.Jeong, K.Suzuki, H.Miura (Tohoku University) /Japan
2. Comparison of Thermal Fatigue Life of SAC Solder Joints and SnPb Solder Joints with Various Stress Ranges
   S.W.R.Lee, C.Yang, Y.S.Chan (Hong Kong University of Science and Technology)/Hong Kong
3. Thermomigration in Eutectic SnPb Solder Joint
   Y.Tao[1], Q.Cheng[1], G,-R.Tang[1], B.Wang[1], B.An[1], F.-S.Wu[1], Y.-P.Wu[1,2] ([1]Huazhong University of Science and Technology, [2]Wuhan National Laboratory for Optoelectronics)/China
4. Concave Shape in Gold-Solder Interconnection System
   J.-Y.Park, E.-J.Choi, S.-C.Lee, Y.-B.Sun (Kyonggi University)/Korea

[15B2-2] Interconnections Ⅱ

1. Development of Ultrasonic Flip-Chip Bonding Interconnection Technologies for COB Modules
   K.Marusaki (Sharp)/Japan
2. Chip-on Flex(COF) Bonding Technology Using Tin Bumps and Non-Conductive Adhesives (NCAs) for CMOS Image Sensor Device
   K.-M.Harr[1], D.-H.Kim[1], Y.-M.kim[1], H.-Y.Cho[1], C.-B.Lee[2], J.-G.Kim[2], S.Yi[2], Y.-H.kim[1] ([1]Hanyang University, [2]Samsung Electro-Mechnics)/Korea
3. Evaluating the Performance of Thermosetting Resins under Ultrasonic Bonding Process
   S.H.Huang[1], H.C.Chen[1], C.L.Chung[1], S.L.Fu[1], S.C.Ho[2], A.H.Liu[2], Y.J.Lee[2] ([1]I-Shou University, [2]ChipMOS Technologies)/Taiwan
4. An Anisotropic Conductive Adhesive Improved by Carbon Nanotubes and Its Application on RFID Tag Inlays Packaging
   X.-H.Cai[1], B.An[1], F.-S.Wu[1], Y.-P.Wu[1,2] ([1]Huazhong University of Science and Technology, [2]Wuhan National Laboratory for Optoelectronics)/China

12:30 13:30 **Lunch time Poster Session**

13:30 **[15B2-3] Interconnections Ⅲ**

1. The Semi-experiment Analysis of the Wire Sweep of a Wire Bond during the Transfer Molding Process
   H.-K.Kung[1], H.-S.Chen[1], H.-C.Hsu[2] ([1]Cheng Shiu University, [2]I-Shou University)/Taiwan
2. Micro-bumping Technology by PPS Method
   K.Tsuruta (Senju Metal Industry)/Japan
3. Flip Chip Assembly on 50-um-pitch Pads Soldered with Precoat by Powder Sheet
   H.Noma (IBM Japan)/Japan
4. Investigation on Wet-Chemical Surface-Cleaning of Au Bump for Low-Temperature Chip Stack-Bonding Using Compliant Bump
   T.Mori[1], N.Watanabe[2], T.Asano[1]([1]Kyushu University, [2]Fukuoka Industry Science & Technology Foundation)/Japan
5. Formation of Micro Au Bump Array for Flip-Chip Bonding using Electroless Au Deposition
   T.Yokosima[1], K.Nomura[1,2], Y.Yamaji[1], K.Kikuchi[1], H.Nakagawa[1], K.Koshiji[1], M.Aoyagi[1,2], R.Iwai[3], T.Tokuhisa[3], M.Kato[3] ([1]National Institute of Advanced Industrial Science and Technology, [2]Tokyo University of Science, [3]Kanto Chemical)/Japan

15:35

15:45 **[15B2-4] Interconnections Ⅳ**

1. Room Temperature Sintering and Bonding with Ag Nanoparticle Paste
   D.Wakuda, K.-S.Kim, K.Suganuma (Osaka University)/Japan
2. Fablication of Large-scale Nanoparticle Array using Combination of Self-assembly and 2-step Transfer
   K.Sugano, T.Ozaki, R.Hiraoka, T.Tsuchiya, O.Tabata (Kyoto University)/Japan
3. Direct Bonding to Aluminum Utilizing Silver-oxide Particles
   Y.Yasuda, E.Ide, T.Morita (Hitachi)/Japan

17:00

17:10 **[15B2-5] Interconnections Ⅴ**

1. Quantitative Measurement of Air-gap of Silicon/Silicon Interfaces
   M.M.R.Howlader, M.G.Kibria, F.Zhang, T. Suga (McMaster University)/Canada
2. Evalution of Electric Contact Phenomena under Small Contact Load
   O.Mukhtar (Osaka University)/Japan
3. True 3D Through Hole Interconnections
   H.Wakioka (Fujikura)/Japan
4. Open Lead Detection Circuit for QFP ICs Using Logic Gates as Open Sensors
   M.Hashizume (University of Tokushima)/Japan

18:50

Room K

[15K-1] Electrical Solutions Ⅰ

1. Effects of Uni-axial Mechanical Stress on the Scattering Parameters of Metal-oxide-semiconductor Field Effect Transistors
   Y.Han[1], M.Koganemaru[2], T.Ikeda[3], N.Miyazaki[3], Y.Kiyotaka[4], W.Choi[4], H.Tomokage[4] ([1]Fukuoka Industry Science & Technology Foundation, [2]Fukuoka Industrial Technology Center, [3]Kyoto University, [4]Fukuoka University)/Japan
2. Bandwidth Simulation for High Speed Memory
   C.-P.Chen, J.-H.Cheng, W.-J.Fan, N.-C.Lin, T.-F.Su (Powertech Technology)/Taiwan
3. Preliminary Study and Design of CMOS Diode for Electrostatic Discharge Protection
   N.F.Muhammad, A.Ibrahim, A.R.Ahmad, M.R.Yahya (Telekom Research & Development) /Malaysia
4. Electrical Characterization of Micro Spring Probe Card for Wafer Level Testing
   H.-Y. Chang (Advanced Semiconductor Engineering)/Taiwan
5. A Target Impedance Profile of Power Distribution System Considering On-Chip Model
   N.Takahashi[1], K.Kagawa[2], K.Hoshino[3] ([1]IBM Japan, [2]ATE Service, [3]Shibaura Institute of Technology)/Japan

(11:05)

(11:15)

[15K-2] Electrical Solutions Ⅱ

1. The Possibility of JISO using Micro Contact
   S.Yoshida, S.Murata, K.Soeta (ALPS Electric)/Japan
2. High-speed Intra-Body Transmission System Using 2 - 28 MHz OFDM Modulation
   F.Koshiji, S.Takenaka, K.Sasaki (The University of Tokyo)/Japan
3. RFID and its Applications in Tourism
   T.Hu (Aizu University)/Japan

12:30 13:30 **Lunch time Poster Session**

13:30 **[15K-3] Mechanical Solutions**

1. Measurement of Three-dimensional Surface Displacement Using the Digital Image Correlation with AFM Images
   N.Shishido, T.Ikeda, N.Miyazaki (Kyoto University)/Japan
2. Multi-angle View Visual Inspection of Solder Joints with Neural Networks
   M.Matsushima (Osaka University)/Japan
3. Package Warpage Simulation Using FEM Visco-Elastic and Cure Degree Coupling
   I.Hirata (NEC)/Japan
4. Numerical Simulation of Variable Frequency Microwave Curing of Underfill Materials
   T.Tilford[1], K.I.Sinclair[2], C.Bailey[1], M.P.Y.Desmulliez[2] ([1]University of Greenwich, [2]Heriot-Watt University)/UK
5. Substrate Trapezoidal Trace Shape Modeling
   L.C.Kim, B.J.Kai (Intel Microelectronic)/Malaysia

15:35

15:45 **[15K-4] Thermal Management Ⅰ**

1. Thermal Design of RGB LED Modules
   A.Andonova, N.Kafadarova (Technical University Sofia)/Bulgaria
2. Comprehensive Thermomechanical Lifetime Calculation of a Soldered Assembly
   G.Massiot, M.Grieu, O.Maire, C.Munier (EADS France)/France
3. Experimental Simulative Analysis for Thermal Performances of Vertical Stacked Die Packages
   C.-K.Yu, C.-K.Liu, S.-L.Kuo, M.-J.Dai, Y.-L.Chao, C.-Y.Hsu, R.-M.Tain (Industrial Technology Research Institute)/Taiwan

17:00

17:10 **[15K-5] Thermal Management Ⅱ**

1. Radiation Cooling Effects on LSI Chip Temerpature with an Alumina Heat Sink of High Infrated Emmisivity Material
   K.Shinagawa[1], M.Nishimura[2], S.Hirokawa[1], Y.Muto[1] ([1]Canon Marketing Japan, [2]NISHIMURA PORCLEAN)/Japan
2. Emissivity Stability Investigation of Substrates and Layers in Microelectronics
   V.Videkov, A.Andonova, N.Kafadarova (Technical University Sofia)/Bulgaria
3. Precursor Monitoring Approach for Reliability Assessment of Cooling Fans
   T.Shibutani[1], H.Oh[2], M.Pecht[2] ([1]Yokohama National University, [2]University of Maryland)/Japan, USA
4. Design and Optimization of 3D Manifold of Microchannel Heat Sink using the Porous Media Approach
   L.F.Yau (Nationa University of Malaysia) /Malaysia

18:50