Advanced Program

ICEP2011

APRIL 13 [Wed] –15 [Fri], 2011

Nara Prefectural New Public Hall, Japan

The International Conference on Electronics Packaging (ICEP) 2011 will be held from April 13th to 15th at the Nara New Prefectural Public Hall in Nara, Japan.

The ICEP2011 conference cover all aspects of the JISSO technologies such as Advanced Packaging, Substrate, Design and Modeling and Reliability, Thermal Management, Manufacturing and Process, Interconnection, Optoelectronics, Printed Electronics, 3D and TSV, MEMS and Sensor, Self-Organization and Self-Assembly, Emerging Technologies, RF, Automotive Electronics, Energy and Environment. The technical program will include five keynote speeches, 46 oral technical sessions and poster sessions. About 200 papers regarding JISSO technologies will be presented by promising researchers from more than 10 countries.

We also plan to hold the welcome events to enjoy the atmosphere of Nara, the old capital city of Japan. People living in Nara are also preparing to welcome all participants with hospitality.

This symposium aims to provide a global forum for presentation and discussion of most recent topics dveloped for the next generation. We expect that ICEP2011 would play an important role not only for understanding fundamental knowledge but also forecasting future technologies to be developed.

We, the organization committee, are confident that the conference will provide excellent opportunities for participants to obtain practical information of technologies and to develop global network. We are looking forwarded to seeing you at the conference.

K. Uenishi

Keisuke UENISHI

General Chairperson of ICEP2011 Committee

Sponsored by:
Japan Institute of Electronics Packaging (JIEP)
IEEE CPMT Society Japan Chapter

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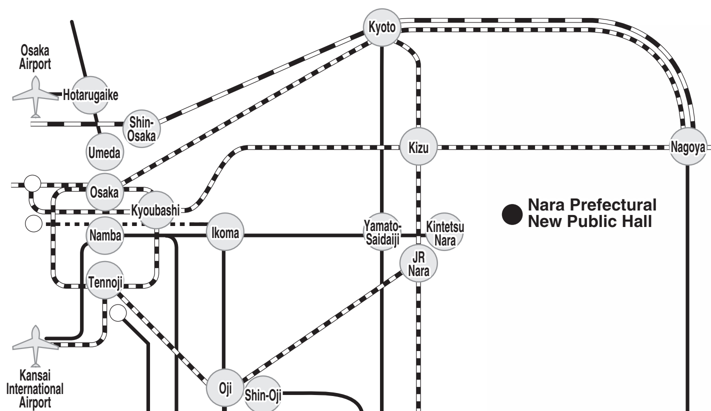
http://www.jiep.or.jp/icep/

Map

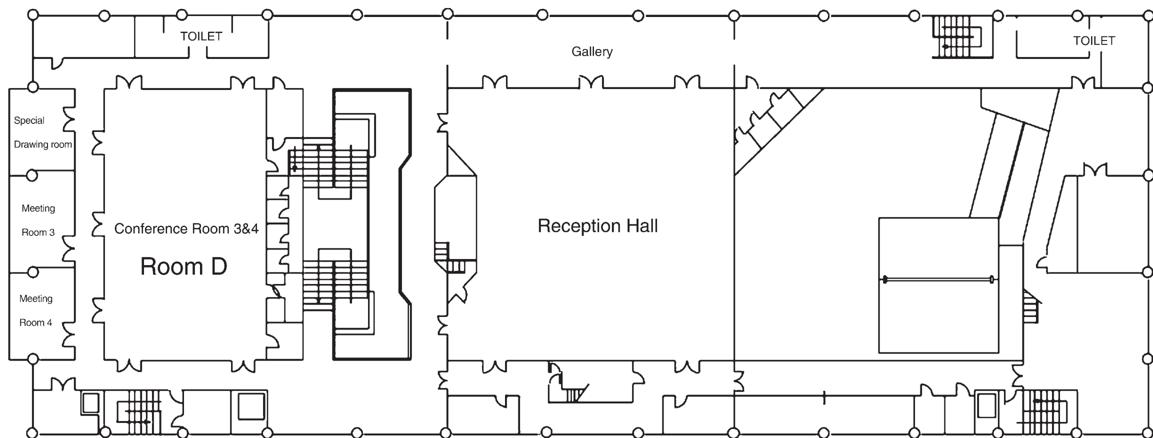


Nara Prefectural New Public Hall

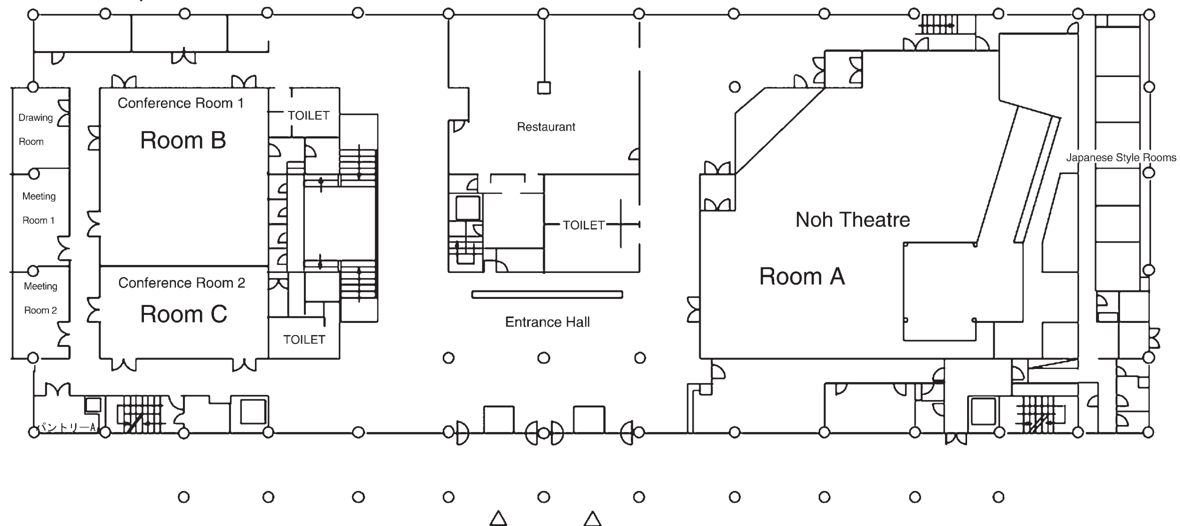
	Room A	Room B	Room C	Room D
10:00 11:15	**WA1: MFG-1** **WA1-1** Analysis on wirebond mechanical integrity of ultra fine pitch wirebond on ultra low-k(ULK) device T.Hisada, T.Aoki, S.Harada, J.C.Malinowski, IBM Japan / Japan **WA1-2** Maximize Memory Capacity Package with Highest Quality and Lowest Cost D.Fann, PowerTech / Taiwan, R.O.C. **WA1-3** Stress Simulation of Underfill Materials in Flip Chip Package T.Sato, Namics / Japan		**WC1: Thermal Management-1** **WC1-1** Electro-Thermal Analysis and Monte Carlo Simulation for Thermal Design of Si Devices T.Hatakeyama[1], M.Ishizuka[1], S.Nakagawa[1], K. Fushinobu[2], [1]Toyama Prefectural University, [2]Tokyo University of Technology / Japan **WC1-2** Electro-thermal scaling analysis of Si MOSFETs with device length typically larger than 100 nm K.Fushinobu[1], T.Hatakeyama[2], [1]Tokyo Institute of Technology, [2]Toyama Prefectural University / Japan **WC1-3** Numerical Study of the Thermal Transfer between Adhesive and CNTs Y.Zhang[1], S.Wang[1], Z.Hu1, J.Liu[1,2], [1]Shanghai University, [2]Chalmers University of Technology / China, Sweden	**WD1: DMR-R-1** **WD1-1** Mechanical and electrical reliability of electroplated copper thin film interconnections N.Murata, N.Saito, F.Endo, K.Tamakawa, K. Suzuki, H.Miura, Tohoku University / Japan **WD1-2** Fracture Strength Characterization of Silicon Die for the Thin Electronic Modules N.Ota, Dai Nippon Printing / Japan **WD1-3** Parametric Study on the BGA Packaging Optimization Y.K.Kim, J.C.Kim, J.Choi, Korea Aerospace University / Korea
11:25 12:40	**WA2: MFG-2** **WA2-1** Development of wafer-level underfill bonding process for 3D chip stacking T.F.Yang, K.S.Kao, J.Y.Chang, C.J.Zhan, Industrial Technology Research Institute / Taiwan, R.O.C. **WA2-2** Process Optimization for Molded Underfill to Reduce Air-trap in a System-in-Package Y.H.Yeh, Y.Amanoand, S.C.Hsu, H.H.Hsu, PowerTech / Taiwan R.O.C. **WA2-3** Effects of Edge and Corner Bonds Underfills on Board Level Shear Strength of Lead-free Package-on-Package Devices H.B.Shi[1,4], Y.Hara[2], F.Ou[3], J.C.Wu[1], T.Ueda[4], [1]Quanta Shanghai, [2]Panasonic Electric Works, [3]Henkel(China), [4]Wasada University / China, Japan	(11:00) **WB2: RF** **WB2-1** The Correlation between Imbalance Component and EM Radiation from a Differential-Paired Line with Different Length Y.Kayano, K.Mimura, H.Inoue, Akita University / Japan **WB2-2** Design and Test of RF Front End for UHF RFID Tag C.C.Huang, K.W.Ku, W.D.Tu, Yuan Ze University / Taiwan **WB2-3** Structural Design of Transmitter and Receiver Electrodes for Improvement of Transmission Characteristics in Human–Body Communi-cation D.Muramatsu, Tokyo University of Science / Japan **WB2-4** An Antenna Apertured with a Half-Semicircle and -Trapezoid in Metal Housing Wall of Electronic Equipments F.Koshiji, K.Koshiji, Tokyo University of Science / Japan	**WC2: Thermal Management-2** **WC2-1** Introduction to Application of Boiling Heat Transfer to High Heat Flux Cooling Technology in Power Electronics K.Suzuki[1], K.Yuki[1], M.Mochizuki[2], [1]Tokyo University of Science, Yamaguchi, [2]Fujikura / Japan **WC2-2** Cooling performance of a two phase (vapor-liquid) flow cooling system M.Chiba, NEC / Japan **WC2-3** Development of High Heat Flux Cooling Jacket for Electronics Devices by using Flow Boiling Y.Shinmoto, Y.Asada, H.Kobayashi, S.Kanazawa, M.Fukagaya, Y.Abe, M.Ouchi, M.Sato, K.Iimura, H.Ohta, Kyushu University / Japan	**WD2: DMR-R-2** **WD2-1** Reliability Desigs for 40 nm ELK Flip-chip Packages with Copper Pillar Bumps Y.S.Lai, M.K.Shih, C.C.Lee, B.K.Appelt, C. Cheung, Advanced Semiconductor Engineering / Taiwan **WD2-2** Investigation of PWB Resin Laminate and Its Relation with the Pad Cratering Resistance S.W.R.Lee, C.Yang, F.Song, Hong Kong University of Science & Technology / China **WD2-3** Determination of Thin-Sisicon Die Strength by Pin-on-Elastic-Foundation Test P.S.Huang, M.Y.Tsai, Chang Gung University / Taiwan R.O.C.
	Lunch			
13:40	**Awarding Ceremony** **Best Paper Awards** **Young Awards**			
14:10 17:20	**Keynote Speeches** **Keynote Speech 1** **Keynote Speech 2** **Keynote Speech 3**			

18:30 20:30	**Welcome Reception**

The second floor plane view



The first floor plane view



	Room A	Room B	Room C	Room D
8:30 10:00	**Keynote Speech** **Keynote Speech 4** **Keynote Speech 5**			
10:10 11:25	**TA1: Korea Session-1** **TA1-1** TBD **TA1-2** TBD **TA1-3** TBD	**TB1: MFG-3** **TB1-1** A New Consortial development approach for Advanced Electronics Packaging B.Bader[1], B.Pfahl[1], H.Fu[2], [1]iNEMI, [2]iNEMI China / U.S.A., China **TB1-2** Proposal of package selection methodology for mobile product J.Asai, T.Hisada, K.Yonehara, IBM Japan / Japan **TB1-3** Investigating the Effects of Area ratio and Aspect ratio Stencil Printing S.Mallik, M.Shafathullah, N.N.Ekere, University of Greenwich / UK	**TC1: DMR-M** **TC1-1** An R&D Informatics Solution towards the Structural and Electronic Properties of Cu Based Intermetallics A.Chatterjee, Accelrys / Japan **TC1-2** Leading Edge eMMC-BGA with Optimized Drop Reliability for Smart Phone Application W.J.Fan, E.Juang, W.Chang, S.Su, Powertech Technology / Taiwan, R.O.C. **TC1-3** Package Design with Extremely Superior 2nd Reliability for SSD Application W.J.Fan, S.Su, E.Juang, W.Chang, Powertech Technology / Taiwan, R.O.C.	**TD1: Advanced PKG-1** **TD1-1** System Packaging by Embedding: Technologies, Examples and Perspectives T.Loeher[1], D.Schuetze[1], A.Ostmann[2], R. Aschenbrenner[2], [1]Technische Universitat Berlin, [2]Fraunhofer IZM / Germany **TD1-2** Matching wire sweep design for 3-demensional and multi-chip module packaging during transfer molding process H.S.Chen, J.C.Hsiung, H.K.Kung, Cheng Shiu University / Taiwan **TD1-3** Next Generation fcCSP Packaging B.K.Appelt, H.Chung, C.Chen, M.Hung, ASE Group / U.S.A., Taiwan
11:35 12:50	**TA2: Korea Session-2** **TA2-1** TBD **TA2-2** TBD **TA2-3** TBD	**TB2: MFG-4** Component Solderability Testing with Board Level Soldering A.Sriyarunya[1], H.Tukiman[2], [1]Spansion(Thailand), [2]Spansion(Kuala Lumpur) / Thailand, Malaysia **TB2-2** Evaluating the effect of pad sizes on the inter-metallic layer formation and growth for Sn-Ag-Cu solders on Cu metallization P.Bernasko[1], S.Mallik[1], N.N.Ekere[1], R.Bhatti[1], G.Takyi[2], [1]University of Greenwich, [2]Kwame Nkrumah University Of Science & Technology / UK, Ghana **TB2-3** Board level reliability Enhancement for a QFN Packaging A.Tseng, M.Lin, B.Hu, JW Chen, JM Wan, S.Lee, Y.S.Lai, ASE(US) / U.S.A.	**TC2: Thermal Management-3** **TC2-1** Heat Transfer Performance of a Micro/Mini Cooling Device using Fins-installed Porous Media for the Next Generation Power Devices K.Yuki, Tokyo University of Science, Yamaguchi / Japan **TC2-2** Liquid Cooling Network System for Energy Conservation in Date Centers M.Ouchi[1], Y.Abe[1], M.Fukagaya[2], H.Ohta[3], Y. Shinmoto[3], M.Sato[4], K.Iimura[4], [1]National Institute of Advanced Industrial Science and Technology, [2]SOHKi, [3]Kyushu University, [4]Utsunomiya University / Japan **TC2-3** Design of a Condensation Section for a Phase Change Cooling System A.Matsunaga, NEC / Japan	**TD2: Advanced PKG-2** **TD2-1** Considerations for 2D Multi-die Fanout Wafer Level Packaging J.Hunt, Advanced Semiconductor Engineering / U.S.A. **TD2-2** Behavior of resin shrinkage in wafer-level packaging using pseudo-SOC technology A.Iida, Y.Onozuka, T.Nagano, H.Yamada, K.Itaya, Toshiba / Japan **TD2-3** Ultra Low Temperature PBO-Polymer for Wafer Level Packaging Applications M.Toepper[1], N.Matsuie[2], T.Motobe[2], T.Minegishi[3], M.Knaus[4], T.Fischer[1], V.Bader[1], K.D.Lang[1], [1]Fraunhofer IZM, [2]HD MicroSystems Japan, [3]Hitachi Chemical, [4]HD MicroSystems Germany / Germany, Japan
	Lunch			
13:35 15:15	**TA3: 3D/TSV-1** **TA3-1** Feasibility Study of a 3D IC Integration System-in-Packaging (SiP) from a 300mm Multi-Project Wafer (MPW) **TA3-2** Wafer Level Packaging of Back Illuminated Image Sensors G.Humpston, M.Kriman, H.Gershtenman-Avsian, Tessera / U.S.A. **TA3-3** Si Interposers with Thick Spiral Inductors for 3D Stacked Buck Converters K.Takemura[1,2], K.Ishida[3], Y.Ishii[1], K.Maeda[1], M. Takamiya[3], T.Sakurai[3], K.Baba[1,2], [1]NEC, [2]Association of Super-Advanced Electronic Technoligies, [3]The University of Tokyo / Japan **TA3-4** Stacking of Known Good Rebuilt Wafers without TSV -Industrial Applications C.Val, P.Couderc, N.Boulay, 3D PLUS / France	**TB3: Thermal Management-4** **TB3-1** Cooling Performance of Compact Finned Heat Sinks under Combined Natural and Forced Convection Air Flows M.Ishizuka, T.Hatakeyama, T.Fukuya, S. Nakagawa, Toyama Prefectural University / Japan **TB3-2** Heart Transfer Correlation of Natural Convection in Square Enclosures with an Inner Object Y.Funawatashi, T.Kita, Toyama Prefectural University / Japan **TB3-3** Improvement of the Thermal Management of Power LEDs by Functional 3D-Substrates with Embedded Fluidic Channels T.Leneke, Otto-von-Guericke-University Magdeburg / Germany **TB3-4** Hybrid Cooling for Fujitsu Large Scale Computing System J.Wei, Fujitsu Advanced Technologies / Japan	**TC3: Optoelectronics-1** **TC3-1** Appication Specific LED Packaging for Automotive Forward-lighting Application F.Chen[1,2], K.Wang[1,2], M.Zhao[1,2], D.Wu[1,2], X. Luo[1,2], S.Liu[1,2], [1]Wuhan National Laboratory for Optoelectronics, [2]Huazhong University of Science & Technology / China **TC3-2** Planar Interconnect for Solder State Lighting and Photonics R.A.Fillion, H.J.Neuhaus, C.E.Bauer, TechLead / U.S.A. **TC3-3** Study on high heat proof protection thin film for Ag reflective films for LED's H.Miyagawa, Osaka University / Japan **TC3-4** A method to decap the LED devices effectively F.Jiao[1,2], R.Cheng[1,2], Q.Zhang[1,2], S.Liu[1,2], [1]Huazhong University of Science & Technology, [2]Wuhan National Laboratory for Optoelectronics / China	**TD3: MEMS-1, BEANS-1** **TD3-1** <Session Invited> BEANS Project based on Multi-Disciplinary Fusion–Process Integration for Hetero-Functional Integrated Devices– M.Takeda[1], A.Yusa[1], H.Fujita[1,2], [1]BEANS Project, [2]The University of Tokyo / Japan (50minutes) **TD3-2** Silicon Microparticle Ejection Using Mist-jet Technology Y.Yokoyama[1], T.Murakami[1], T.Tokunaga[1], T. Itoh[1,2], [1]BEANS Project, [2]AIST / Japan **TD3-3** Continuous high speed thin film coating process on fiver-type substrates with die coater N.Shibayama[1], S.Takamatsu[1], T.Itoh[1,2], [1]BEANS Project, [2]AIST / Japan
15:25 17:05	**TA4: 3D/TSV-2** **TA4-1** Development of 5µm Diameter Backside Cu TSV Technology for 3D LSI Y.Ohara, Y.Watanabe, K.Lee, T.Fukushima, M. Koyanagi, T.Tanaka, Tohoku University / Japan **TA4-2** Improvement of the nonlinear finte element analyses for 3D SIC using the strain measurement by the digital image correlation T.Ikeda, S.Kawahara, M.Oka, N.Miyazaki, Kyoto University **TA4-3** Thermo-mechanical Stress Analysis of Though Silicon Via (TSV) by Finite Element Method D.S.Liu[1], C.Y.Tu[1], S.S.Yeh[1], H.Y.Chen[1], A.H.Liu[2], [1]National Chung Cheng University, [2]ChipMos Technologies / Taiwan R.O.C. **TA4-4** Reliability characterization of 20 µm pitch microjoints assembled by a conventional reflow technique T.C.Chang, R.S.Cheng, P.C.Chang, Y.P.Hung, J.Y.Chang, T.F.Yang, S.Y.Huang, Industrial Technology Research Institute / Taiwan, R.O.C.	**TB4: Thermal Management-5** **TB4-1** High Thermal Conductivity Multilayer Nanofilms for Reducing Thermal Hot Spots in LSI devaices F.Kato[1], K.Kikuchi[1], M.Aoyagi[1], T.Iwashita[2], H.Fujiwara[2], [1]National Institute of Advanced Industrial Science and Technology, [2]Furukawa Electric / Japan **TB4-2** Thermal Simulations and Measurements – a Combined Approach for Package Characterization A.Vass-Varnai, R.Bornoff, Y.Luo, A.Poppe, G. Farkas, M.Rencz, Mentor Graphics / Hungary **TB4-3** Transient Heat Conduction Simulation of the Lidless Micro PGA Processor K.Nishi, AMD Japan / Japan **TB4-4** On Effective Thermal Conductivity of Electronic Wiring Board Y.Koito, T.Tomimura, Kumamoto University / Japan	**TC4: Optoelectronics-2** **TC4-1** Low-loss chip assembly for low-power optical I/O on waveguide - integrated organic carrier M.Tokunari, Y.Tsukada, K.Toriyama, H.Noma, S.Nakagawa, IBM Japan / Japan **TC4-2** Surface activated bonding of optical chips using Au stud bumps for optical microsensor applications T.Sato, The University of Tokyo / Japan **TC4-3** Spherulites Investigative of Poly (9,9-di-n-octy1-2,7-fluorene) (PFO) J.K.Ke, C.L.Chung, Y.J.Huang, S.L.Fu, I-Shou University / Taiwan, R.O.C. **TC4-4** Photovoltaic Devices Using Electrospun Semi-conductive Polymer J.K.Ke, C.L.Chung, S.L.Fu, I-Shou University / Taiwan, R.O.C.	**TD4: MEMS-2, BEANS-2** **TD4-1** Formation of Organic Crystalline Nanopillar Arrays and Their Application to Organic Photovoltaic M.Hirade[1,2], H.Nakanotani[1,2], M.Yahiro[1,2,3], C. Adachi[1,2,3], [1]BEANS Project, [2]Kyushu University, [3]Institute of Systems, Information Technologies and Nanotechnologies / Japan **TD4-2** Formation of organic semiconducting nano-dots by using vacuum deposition process and application for organic solar cells M.Nakata[1,2], K.Kawano[1,2], M.Yasumatsu[1,3], M.Yahiro[1,4], C.Adachi[1,3,4], 1BEANS Project, [2]Panasonic Electric Works, [3]Kyushu University, [4]Institute of Systems, Information Technologies and Nanotechnologies / Japan **TD4-3** Preparation of porous film at micro-scale and nano-scale by modified breath figure method Y.Zheng[1,3], Y.Kubowaki[2], K.Miyazaki[1,2], C. Adachi[1,3], [1]BEANS Project, [2]Kyushu Institute of Technology, [3]Kyushu University / Japan **TD4-4** Minimizing Etching Damages of Organic Semiconductor Layers by Neutral Beams J.Adachi[1,2], T.Kubota[1,3], M.Yahiro[1,4], S. Sakukawa[1,5], C.Adachi[1,2], [1]BEANS Project, [2]Kyushu University, [3]The University of Tokyo, [4]Institute of Systems, Information Technologies and Nanotechnologies, [5]Tohoku University / Japan
17:15 18:30	**TA5: Interconnection-1** **TA5-1** Effect of oxygen partial pressure on sintering nanoscale silver die-attachment on copper substrate H.Zheng, Virginia Polytechnic Institute and State University / U.S.A. **TA5-2** Natural Rubber-g-PVP/Silver Nanocmposites as Potential Conductive Adhesives N.H.H.Abu Bakar, J.Ismail, M.Abu Bakar, S. Yaakob, Universiti Sains Malaysia / Malaysia **TA5-3** Bondability of Low Temperature Sinter Bonding Using Ag2O Pastes with Polyethylene Glycols T.Yagishita, T.Ogura, A.Hirose, Osaka University / Japan	**TB5: MFG-5** **TB5-1** Eco-fabircation of noble metal nanoparticle related materials by liquid-solid reaction Y.Hayashi, Tohoku University / Japan **TB5-2** Aerosol Jet Printing and Rapid Protoyping Methods for Flexible Structuring of 3D C.Goth, S.Putzo, J.Franke, University of Erlangen-Nuremberg / Germany **TB5-3** Fabrication and application of Ag nanoparticles by ultrasonic process D.Ishikawa[1], T.Abe[1], K.Toisawa[2], Y.Hayashi[2], H. Takizawa[2], [1]Hitachi Cable, [2]Tohoku University / Japan	**TC5: Automotive** **TC5-1** Shrinkage and Sintering Behavior of a Low-Temperature Sinterable Nanosilver Die-Attach Paste T.Wang[1,2], M.Zhao[1], X.Chen[2], G.Q.Lu[1,2], K.Ngo[1], S.Luo[3], [1]Virginia Tech, [2]Tianjin University, [3]NBE Technologies / U.S.A., China **TC5-2** Low-Temperature Sintering of Nanoscale Silver Paste for Attaching Large-Area Silicon Devices K.Xiao, J.Calata, G.Q.Lu, Virginia Polytechnic Institute and State University / U.S.A. **TC5-3** Thermal expansion behavior of Cu6Sn5 in high temperature lead-free solder joints D.Mu, J.Read, Y.F.Yang, K.Nogita, The University of Queensland / Australia	**TD5: MEMS-3, BEANS-3** **TD5-1** Site-Slective Binding of Nanoparticles onto a Silicon Chip by Peptides with an Affinity for Inorganic Materials Y.Shimada[1,2], M.Suzuki[1], M.Sugiyama[1,2], I. Kumagai[3], M.Umetsu[1,3], [1]BEANS Project, [2]The University of Tokyo, [3]Tohoku University / Japan **TD5-2** Damage-free silicon etching using large diameter neutral beam source T.Kubota[1,2], S.Ueki[1], Y.Nishimori[1], G. Hashiguchi[1,3], M.Sugiyama[1,2], S.Samukawa[1,4], [1]BEANS Project, [2]The University of Tokyo, [3]Shizuoka University, [4]Tohoku University / Japan **TD5-3** Embedded Nano-channel Fabricated in Fused Silica by Femtosecond Laser Irradiation and Wet Etching for Nano-scale Fluid Devices O.Nukaga[1], S.Yamamoto[2], K.V.Tabata[1,3], T. Kubota[1,4], S.Samukawa[1,5], M.Sugiyama[1,4], [1]BEANS Project, [2]Fujikura, [3]Osaka University, [4]The University of Tokyo, [5]Tohoku University / Japan

	Room A	Room B	Room C	Room D
8:30 10:10	**FA1: Interconnection-2** **FA1-1** <Session Invited> Advanced Packaging the New Decade E.J.Vardaman, TechSearch International / U.S.A. **FA1-2** C2 assembly on gold plated pads H.Noma, K.Toriyama, K.Matsumoto, E.Ohno, H. Mori, Y.Orii, IBM Japan / Japan **FA1-3** A study of underfill materials for reliability impronement fc-PKG Y.Muranaka, Sanyu Rec / Japan **FA1-4** Chip Package Interaction Study for Large Flip Chip Ball Grid Array with Cu/low-k on-chip interconnect C.Uchibori, Fujitsu Laboratories America / U.S.A.	**FB1: Substrate-1** **FB1-1** Preparation and characterization of PBS-Al2O3 glass-ceramics for LTCC applications C.S.Mahmood[1], A.Ibrahim[2], M.H.Al Rashid Megat Ahmad[1], N.U.Saidin[1], R.Alias[2], [1]Malaysia Nuclear Agency, [2]Lingkaran Teknokrat Timur / Malaysia **FB1-2** Patterning of Different Materials Inside LTCC Green Sheet Using Photo Resist Film M.Takatou, Nihon University / Japan **FB1-3** The Electroless Ni-P Plating Film Adapting for Flexible Printed Wiring Boards Y.Tanabe, Okuno Chemical Industries / Japan **FB1-4** Surface modification of polyimide by 172 nm excimer lamp irradiation T.Kasahara, H.Shinohara, S.Shoji, J.Mizuno, Waseda University / Japan	**FC1: MFG-6** **FC1-1** Optimization of cyclo-olefin polymer-polydimethylsiloxane direct bonding conditions for biochemical microchips A.Nakahara, H.Shinohara, T.Kasahara, S.Umeda, S.Shoji, J.Mizuno, Waseda University / Japan **FC1-2** Single diallylamine type copolymer additive which perfectly bottom-up fills Cu electrodeposition M.Takeuchi[1], K.Kondo[2], H.Kuri[2], M.Bunya[1], N. Okamoto[2], T.Saito[2], [1]Nitto Boseki, [2]Osaka Prefecture University / Japan **FC1-3** Die pull tester for flip-chip bonding Y.Arai, Toray Engineering / Japan	**FD1: Printed-1** **FD1-1** <Session Invited> RecentProgess in Research Development of Printed TFT Technology T.Kamata, National Institute of Advanced Industrial Science and Technology / Japan (50 minutes) **FD1-2** <Session Invited> Ink-jet printed Cu metal pattern cured at room temp. using UV+IR light J.Novak, AppliedNanotech / U.S.A. (50minutes)
10:20 12:00	**FA2: Interconnection-3** **FA2-1** Highlight of 2011 iNEMI Technology Roadmap M.Tsuriya, C.Richardson, R.C.Pfahl,Jr., H.Fu, International Electronics Manufacturing Initiative / U.S.A. **FA2-2** An Experimental and Numerical Investigation into the Optimal Au-Sn Bonding Temperature Conditions for Chip-On-Film Packages D.S.Liu[1], S.S.Yeh[1], C.Y.Tu[1], C.I.Tsai[2], A.H.Liu[2], C.T.Kao[3], [1]National Chung Cheng University, [2]ChipMos Technologies, [3]Spatial Photonics / Taiwan R.O.C., U.S.A. **FA2-3** Development of Fine-Pitch Flip Chips Assembly on Flexible Printed Circuits Y.Amemiya, Fujikura / Japan **FA2-4** Effects of Intermetallic Compound Thickness on Solder Bump Reliability of High-density 3D Chip-to-chip Interconnect Technology H.C.Cheng[1], Y.M.Tsai[2], S.T.Lu[2,3], W.H.Chen[2], [1]Feng Chia University, [2]National Tsing Hua University, [3]ITRI / Taiwan, R.O.C.	**FB2: Substrate-2** **FB2-1** Development of Thermal Management on LSI Embedding Multi-Layer Printed Wiring Board S.Amakai, Dai Nippon Printing / Japan **FB2-2** Cu-BaTiO$_3$-epoxy Composites with High Permittivity for Embedded Capacitors S.Yu, S.Luo, R.Sun, Chinese Academy of Sciences / China **FB2-3** Release Process of the Ferroelectric films and Its Applications F.Tomioka, The University of Tokyo / Japan **FB2-4** Electrical insulator material with ultralow CTE H.Deguchi, Sekisui Chemical / Japan	(9:55) **FC2: DMR-E-1** **FC2-1** Accurate High-Frequency Substrate Modeling and Its Characterization for Multi-Gbps Serial Link I/O J.Kong, J.K.Beh, C.K.Lee, Intel Micronics / Malaysia **FC2-2** An Optimization Study on High-Frequency Vertical Interconnect J.Kong, J.K.Beh, J.Wong, Intel Micronics / Malaysia **FC2-3** Integrated power delivery analysis thorught power rail merging sceme Y.H.See Tau, Intel Microelectronics / Malaysia **FC2-4** Analysis of DDR3 Full Channel Performance Impact Caused by Routing Over Package PTH Void J.K.Beh, Intel Micronics / Malaysia **FC2-5** An In Depth Study of Gen3 High Speed Differential I/O Routing Over Active PTH with Induced Crosstalk C.K.Lee, J.K.Beh, F.Phun, Intel Microelectronics / Malaysia	**FD2: Printed-2** **FD2-1** High Performance of Inkjet Printhead for Printed Electronics Applications S.Nishi, Konicaminolta IJ Technologies / Japan **FD2-2** Ag/Cu Bimetallic Nanoparticle Inks for Wiring and Bonding M.Nakamoto[1], T.Nagaoka[1], Y.Morisada[1], M. Yamamoto[1], Y.Kashiwagi[1], M.Fukusumi[1], T.Ohno[1], H.Kakiuchi[2], Y.Yoshida[2], [1]Osaka Municipal Technical Research Institute, [2]Daiken Chemical / Japan **FD2-3** Development of Transparent Conductive Films by the Use of Metal-oxide Nanoparticle Pastes K.Murahashi, Okuno Chemical Industries / Japan **FD2-4** Manufacture of Silver Nanopartilces for Electro-conductive Application R.H.Jin, DIC / Japan
	Lunch			
13:00 14:40	**FA3: Interconnection-4** **FA3-1** Solder Bumping and Processing of Flip-Chips with a Solder Bump Diameter of 30 µm or 40µm T.Oppert[1], R.Dohle[2], F.Schubler[3], J.Franke[3], [1]Pac Tech Packaging Technologies, [2]Micro Systems Engineering, [3]University of Erlangen-Nuremberg / Germany **FA3-2** Flip-chip Interconnection by Nanoparticle Deposited Cone-bumps for Heterogeneous Multi-chip-stacking Cool Systems F.Imura[1], S.Nemoto[1], F.Kato[1], K.Kikuchi[1], M. Suzuki[1], H.Nakagawa[1], M.Aoyagi[1], H.Uchida[2], M.Hagimoto[2], M.Chacin[2], T.Miyazaki[2], T. Ohkawa[2], R.Ikemo[2], Y.Matsumoto[2], [1]National Institute of Advanced Industrial Science and Technology, [2]TOPS Systems / Japan **FA3-3** Observation of Micro Solder Bump Replication Phenomena by High Speed CCD K.Yasuda, N.Amemori, O.Takai, Nagoya University / Japan **FA3-4** Technology of fluxless polymer for solder-on-pad (SoP) K.S.Choi, K.H.Yoo, J.T.Moon, Y.S.Eom, ETRI / Korea	**FB3: MEMS-4** **FB3-1** Bonding properties of low-temperature wafer bonding using sub-micron Au particles for MEMS hermetic packaging H.Ishida[1], T.Ogashiwa[2], S.Ishizuka[3], T.Yazaki[1], Y.Kanehira[2], T.Nishimori[2], J.Mizuno[3], [1]SUSS MicroTec, [2]Tanaka Kikinzoku, [3]Waseda University / Japan **FB3-2** Hybrid MEMS manufacturing using micro-electronics packaging technoligies G.P.Li, M.Bachman, University of California / U.S.A. **FB3-3** A Novel Biocompatible Direct Bonding Technique for Class Microdevaices C.Wang[1], Y.Xu[1], J.Umeda[1], Y.Dong[2], K.Mawatari[1], T.Kitamori[1], T.Suga[1], [1]The University of Tokyo, [2]Chinese Academy of Inspection and Quarantine Science / Japan, China **FB3-4** Hermetic packaging for optical microsystems by Au-Au surface activated bonding in ambient air S.Yamamoto[1], E.Higurashi[1], T.Suga[1], R.Sawada[2], [1]The University of Tokyo, [2]Kyushu University / Japan	**FC3: DMR-E-2** **FC3-1** Identification of Interconnect Degration using Nonlinearity Measurement Techniques M.Kruger[1], N.F.Nissen[2], H.Reichi[1], K.D.Lang[1], [1]Technische Universitat Berlin, [2]Fraunhofer Institute for Reliability and Microintegration / Germany **FC3-2** Fault Analysis of Soft Open Defects in TSVs with Electromagnetic Simulator M.Hashizume, The University of Tokusima / Japan **FC3-3** A Dual Channel Defect Position Identification Method for Touch Panel Manufacturing Process H.Hamori, M.Sakawa, H.Katagiri, T.Matsui, Hiroshima University / Japan **FC3-4** Estimation of Faulty Effects Caused by a Clack at an Interconnect Line in 90nm ICs K.Manabe, Kagawa National College of Technology / Japan	**FD3: Printed-3** **FD3-1** Material Technology of Conductive Wiring by Ink-jet Print M.Inada, Y.Kumashiro, H.Nakako, T.Noudou,K. Kuroda, K.Yamamoto, Hitachi Chemical / Japan **FD3-2** Chisso's Printing Materials for Printed Electronics H.Anraku, Chisso Petrochemical / Japan **FD3-3** High Performance Inkjet System S-200 S.Iguchi, ULVAC / Japan **FD3-4** The New CAD to BMP Transformation Software M.Oda[1], K.Yamamoto[2], [1]ULVAC, [2]ZUKEN / Japan
14:50 16:30	**FA4: Interconnection-5** **FA4-1** Effect of Nickel Addition on the Interfacial Reactions between Sn-3Ag-0.5Cu Solders and Immersion Silver Surface Finishes I.Siti Rabiatull Aisha[1], A.Ourdjini[1], O.Safoura[1], Y.T.Chin[2], [1]University of Technology Malaysia, [2]Intel Technology / Malaysia **FA4-2** Influence of UBM Layers on Electro-migration Behavior of Micro-joints using Sn-Ag Solders D.Toyoshima, K.Yasaka, T.Sakai, T.Akamatsu, N.Imaizumi, S.Sakuyama, K.Uenishi, Osaka University / Japan **FA4-3** Computation Study on the Mechanical Properties and Electromigration in Nanoscale Cu/Sn/Cu and Cu/Sn-Bi/Cu Solder Joints S.Xu, Y.C.Chan, Q.Li, S.Ismathullakhan, City University of Hong Kong / Hong Kong **FA4-4** Effects of heat treatment on Kirkendall void formation at Cu/Sn-3.5Ag solder joint S.H.Kim, J.Yu, KAIST / Japan	**FB4: MEMS-5** **FB4-1** Development of micro-coolers using thermo-electric materials L.L.Liao, Industrial Technology Research Institute / Taiwan R.O.C. **FB4-2** Signficance of a priori prediction of encountered stresses during fabrication of smart monolithic sensor devices and packaging A.Matin, K.Oishi, T.Sugai, D.Akai, K.Sawada, M.Ishida, Toyohashi University of Technology / Japan **FB4-3** Formation of glass nano particles using electrospinning method K.Uchida, N.Miki, Keio University / Japan **FB4-4** Liquid encapsulation to MEMS and its application to a micropump K.Nakahara, Keio University / Japan	**FC4: DMR-E-3** **FC4-1** Performance Enhancements for Multi-Die DRAM Packages R.Crisp[1], W.Zohni[1], B.Haba[1], D.Fann[2], W.Chang[2], A.Chang[2], [1]Tessera, [2]PowerTech / U.S.A., Taiwan R.O.C. **FC4-2** The multiple signal reflection cancellation design technique for high-speed transmission line in low-cost wire-bonding BGA packages T.Tsukuda, K.Hotta, S.Nisizono, Renesas Electronics / Japan **FC4-3** Effect of PDN Impedance Change on Gbps Signal Propagation Using Decoupling Capacitor Embedded Interposer for 3D-Integrated LSI System K.Kikuchi[1], K.Shimakura[2], K.Takemura[2], T. Gomyo[2], T.Ookubo[2], T.Koyama[2], T.Murakami[2], M.Aoyagi[1], K.Otsuka[3], [1]National Institute of Advanced Industrial Science and Technology, [2]Association of Super-Advanced Electronic Technologies, [3]Meisei University / Japan **FC4-4** A New Approach for Higher Level of Power Integrity on Circuit Boards N.Sasaoka[1], T.Ochi[1], K.Otsuka[2], [1]Nippon Kodoshi, [2]Meisei University / Japan	**FD4: Printed-4** **FD4-1** Printed Organic TFT for Flexible Devices H.Maeda, Dai Nippon Printing / Japan **FD4-2** Pico liter dispenser with needle and tube for repair systems Y.Kato, Applied Micro Systems / Japan **FD4-3** The size effect in the resistivity of the narrow printed tracks C.J.Kim, M.Nogi, K.Suganuma, Osaka University / Japan (16:05) (16:15) **FD4-4** Advancement of device prototyping and fabrication techniques for sensors and flexible electronics J.L.Zunino, D.P.Schmidt, A.M.Petrock, B.E.Fuchs, US Army Armament Research Development & Engineering Center / U.S.A. **FD4-5** Shapeable Li-ion Batteries as Substrate: Printed Electronics Reliability N.B.Palacios-Aguilera[1], U.Balda-Irurzun[3], A. Sridhar[3,4], J.Bastemeijer[1], J.R.Mollinger[1], R. Akkerman[3], J.Zhou[2], P.J.French[1], A.Bossche[1], [1]Delft University of Technology, [2]Philips Research Europe, [3]University of Twente, [4]Fraunhofer ENAS / The Netherlands, Germany **FD4-6** Work Function Control for Printed Pattern Using Pressure Annealing Technique M.Yoshida, K.Suemori, S.Uemura, S.Hoshino, N.Takada, T.Kodzasa, T.Kamata, National Institute of Advanced Industrial Science and Technology / Japan (17:30)
16:40 18:20	**FA5: Interconnection-6** **FA5-1** Improvement of brittleness of pure Zn by addition of minor elements as high temperature lead-free solder S.W.Park, K.S.Kim, K.Suganuma, Osaka University / Japan **FA5-2** Influence of Zn Addition to Eutectic Sn-Bi Solder on Joint Reliability with Cu Electrode T.Akamatsu, Fujitsu Laboratories / Japan **FA5-3** The Development of an Improved Tin-Zinc Solder K.Sweatman, T.Nozu, T.Nishimura, Nihon Superior / Japan **FA5-4** Whisker Formation on Lead-Free Tin-Copper plating by Mechanical Stress Y.Mizuguchi, Sony / Japan	**FB5: MEMS-6** **FB5-1** Fabrication and thermal design of a two directional electrostatic comb-drive actuator for capacitive sensing S.C.Choi, Advanced Industrial Science and Technology / Japan **FB5-2** Development and Design of Self-Breathing Micro Fuel Cells for Autonomous Portable Applications M.Weiland[1], S.Wagner[2], R.Hahn[2], H.Reichl[1], [1]Technische Universitat Berlin, [2]Fraunhofer Institute for Reliability and Microintegration / Germany **FB5-3** Thik Film Resistors on Stainless as Sensing Elements for Strain Sensor Applications Z.Zhang[1,2,3], J.Chen[3], C.Liu[2], G.Cao[2], B.Song[3], S.Liu[1,2], [1]Wuhan National Laboratory for Optoelectronics, [2]Huazhong University of Science & Technology, [3]FineMEMS / China	**FC5: DMR-E-4** **FC5-1** A High Signal-Integrity PCB-Trace Composed of Multiole Segments for VLSI Packaging in GHz Domain M.Yasunaga[1], H.Shimada[1], S.Akita[1], M.Ishiguro[1], I.Yoshihara[2], [1]University of Tsukuba, [2]Miyazaki University / Japan **FC5-2** A Novel Magnetic Shield Structure for MRAMs with Perpendicular Magnetic Anisotropy T.Watanabe[1], T.Manako[2], S.Yamamichi[1], [1]Renesas Electronics, [2]NEC / Japan **FC5-3** Study on Wiring Characteristics for Isostatic Conductive Paste K.Hashimoto[1], Y.Akiyama[1], K.Kohno[1], K.Otsuka[1], K.Suganuma[2], M.Takeuchi[3], [1]Meisei University, [2]Osaka University, [3]Uni-Science Takeuchi / Japan **FC5-4** System Model Visualization Method for 3D-SiP H.Murata, Osaka University / Japan	

Poster Session

No.	Title / Authors
P001	Monitoring method of residual stress in a substrate during thin film processing K.Nakahira, H.Tago, H.Kishi, K.Suzuki, H.Miura, Tohoku University / Japan
P002	Direct Copper Electrodeposition on High Resistivity substrates from Ethylenediamine Complex bath H.Arimura[1,2], [1]Konan University, [2]Ishihara Chemical / Japan
P003	All-Wet Cu-TSV Fabrication Process Using Electroless Barrier and Seed Layers R.Arima[1], F.Inoue[1], T.Yokoyama[1], H.Miyake[1], S.Tanaka[2], T.Terui[2], T.Shimizu[1], S.Shingubara[1], [1]Kansai University, [2]National Institute of Information and Communication Technology / Japan
P004	Adsorption and desorption kinetic study of organic additives during copper electrodeposition by microfluidic reactor Y.Miyamoto, S.Hattori, N.Okamoto, T.Saito, K.Kondo, Osaka Prefecture University / Japan
P005	Stress-induced migration of the electroplated copper thin film interconection N.Saito, N.Murata, K.Tamakawa, K.Suzuki, H.Miura, Tohoku University / Japan
P006	Modeling the process window of Bond Line Thickness for Printable Die Attach Adhesives in DRAM wBGA packaging C.H.Lu, W.F.Chang, Powerchip Technology / Taiwan, R.O.C.
P007	Effects of Laser Irradiation Conditions on Bonding Characteristics of Lead-free Solder Joints by Laser Soldering N.Iwata, Osaka University / Japan
P008	Reliability Evaluation for Cell Bonding in Slat-type Soler Module N.Atsuta, Toray Engineering / Japan
P009	Effect of Learning Pseudo Defective Samples Generated with Charactaristic Vector in Neuro Visual Inspection System N.Nakashima, Osaka University / Japan
P010	Effect of thermal/humidity stress on the reliability of high power blue LEDs S.Zhou[1], Q.Zhang[2], S.Liu[1,2], [1]Shanghai Jiao Tong University, [2]Huazhong University of Science & Technology / China
P011	Simulation and Experiments on the Performance of LED under Temperature Shock X.Gui[1,2], X.Luo[1,2], S.Liu[1,2], [1]Wuhan National Laboratory for Optoelectronics, [2]Huazhong University of Science & Technology / China
P012	Wavelength Addressing Optical Interconnection Using Plug-in Alignment with A Multi-Way Optical Socket K.Nakama, Tokai University / Japan
P013	Modeling and Characterization of Packing Power Delivery System with Embedded Discrete Capacitors H.H.Cheng[1], C.W.Kuo[1], P.C.Pan[2], C.Y.Huang[2], C.C.Wang[2], C.T.Chiu[2], [1]National Sun Yat-Sen University, [2]Advanced Semiconductor Engineering / Taiwan
P014	A study of Cable Failure Diagnosis Using TDR T.Kuwahara, Mitsubishi Electric / Japan
P015	A Low Power Consumption QVCO Design for RF Package Effect Validating S.M.Wu, R.S.Huang, B.H.Yu, National University of Kaohsiung / Taiwan, R.O.C.
P016	Novel Substrate Design Kit with Power Delivery System Resonant for RF Package Signal Integrity S.M.Wu, M.H.Li, C.T.Kuo, National University of Kaohsiung / Taiwan, R.O.C.
P017	An Experimental Study of Planar-scanning Near-field to Far-field Transformation using a Dipole Zntenna T.Watanabe[1], J.Ochiai[1], K.Takizawa[2], H.Kurihara[2], O.Hashimoto[1], [1]Aoyama Gakuin University, [2]TDK-EPC / Japan
P018	Study on Hierarchal Optimization Method in Design of System LSI T.Yasumura, Osaka University / Japan
P019	Quic Changeover Approach Test Handler C.S.Chew, N.R.Subramanian, Intel Technology / Malaysia
P020	Deposition of copper particles onto porous silicon: Morphological transformation from cube to spherical shape particles M.A.Bakar, S.Yaakob, W.L.Tan, J.Ismail, K.Ibrahim, University Sains Malaysia / Malaysia
P021	Thermal behaviour and kinetic study of the thermal degradation of ENR-based polyelectrolytes W.L.Tan, M.A.Bakar, University Sains Malaysia / Malaysia
P022	Electrical and thermal conductivities of thermally conductive adhesives composed of a multi-functional epoxy resin containing Cu fillers coated with Ag M.Inoue[1], H.Muta[1], S.Yamanaka[1], J.Liu[2,3], [1]Osaka University, [2]Chalmers University of Technology, [3]Shanghai University / Japan, Sweden, China
P023	Using wet etching process and electroless nickel plating process to fabricate CMOS-MEMS probe chip K.Y.Lee, J.T.Huang, H.J.Hsu, C.K.Chen, T.C.Tsai, National Taipei University of Technology / Taiwan, R.O.C.
P024	Electroformed Printing Pins H.J.Hsu, J.T.Huang, K.Y.Lee, T.C.Tsai, National Taipei University of Technology / Taiwan, R.O.C.
P025	Three-dimensionnal Micro Fluidics Device Using Contrifgal Force T.Azeta[1], Y.Ukita[2], H.Nose[1], S.Kondo[1], Y.Utsumi[1], [1]University of Hyogo, [2]Japan Advanced Institute of Science and Technology / Japan
P026	High-sensitive enzyme-linked immunosorbent assay in three-dimensional lab-on -a-chip T.Azeta[1], Y.Ukita[2], H.Nose[1], S.Kondo[1], Y.Utsumi[1], [1]University of Hyogo, [2]Japan Advanced Institute of Science and Technology / Japan
P027	High-Sensitive Detection of Polychlorinated Biphenyl on Three-Dimensional Lab-on-a-CD H.Nose[1], T.Azeta[1], Y.Ukita[2], S.Kondo[1], C.Kataoka[3], Y.Utsumi[1], [1]University of Hyogo, [2]Japan Advanced Institute of Science and Technology, [3]Carbuncle Baioscientech / Japan
P028	Proposal of stacked electrodesfor multiplex neural interface M.Yoshida, University of Hyogo / Japan
P029	A biochip using antibody-covered magnetic particles to detect the concentration and antibiotics resistance of specific bacteria J.T.Huang, C.C.Hsieh, G.C.Wang, National Taipei University of Technology / Taiwan, R.O.C.
P030	Blood vessel pressure sensor measurement using the CMOS-MEMS technique J.T.Huang, H.R.Jan, National Taipei University of Technology / Taiwan, R.O.C.
P031	Study and Development on the Flexible Pressure-sensor Composed of Nano composite Materials J.T.Huang, C.C.Cheng, S.C.Lan, National Taipei University of Technology / Taiwan, R.O.C.
P032	Mechanical and Electrical Properties of Self-Restoring Sheet Materials for Stretchable Circuits N.Sekido, K.Yasuda, O.Takai, Nagoya University / Japan

Oral Session

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