Sample

35 mm

Size A4

Organic Build-up Package for Fine Pitch High Pin Count Chip Application

Paper Title

1 line space

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Abstract

A build up package consisting of PPE resin (Poly-Phenylene Ether) was developed to mount high pin count chips using flip chip technology. The package was designed to mount 250 ?m full grid array chips, therefore the design rule is as follows, line and space are 45 ?m, via and via land diameter are 50 ?m and 110 ?m respectively. The reliability result obtained by environmental tests showed that the package satisfied all the requirements because a resin used as core and build up dielectric layer is PPE resin which has good moisture stability, low dielectric constant and proper CTE (Coefficient of Thermal Expansion). This paper describes the property of PPE resin, package structure, fabrication process, design and evaluation results of the package.

23 mm

23 mm

Abstract (1 column)

230 mm

7 mm

163 mm

Introduction

Recently performance of semiconductor chip has been improved remarkably and number of I/O terminal and clock frequency are rapidly increasing mainly in microprocessors and ASICs[1]. To assemble such a high pin count chips on package, flip chip interconnect has been introduced.

The package material is changing from ceramic to plastic due to better CTE matching with mother board, lower trace resistance and lower dielectric constant to transmit high frequency signals[2]. However reliability issues have been big concern to use plastic materials for packages. Recently various kinds of plastic materials have been offered from material suppliers, therefor wider material selection has been developed and proper material selection for low end, middle end and high end application is available. In the near future, high performance chips will appear and need superior materials for GHz level signal transmission[3].

In package manufacturing technology, build up process for PCB becomes more popular because it is easy to make fine circuit patterns. In this process, there are two kinds of methods to make via in insulation layers, one is photo via process using photo imaginable resin, another is laser via process using thermosetting resin. The photo process has advantage for mass production ability at low cost, but it lacks for flexibility to modify resin property because photo functional group must exist in resin matrix , on the other hand laser process has advantage for easy modification of resin property but production ability should be improved[4]. In this study we selected a laser via process to satisfy tough reliability requirements in comparison with existing materials.

Among various kinds of resins, PPE has attractive properties such as low water absorption and low dielectric constant, therefore we chose this material as candidate for packages and tried to modify the properties. PPE resin was improved to get proper CTE and young modulus for build up dielectric layers. (PPE resin has been supplied from Asahi Chemical.)

A build up package consisting of this PPE was developed and applied to a high pin count flip chip application. The reliability results obtained by environmental tests were satisfactory. The package structure, process, resin property, design rule and reliability are described.

Text (2 columns)

Package structure and process

Package structure

Build up layers are laminated on core consisting of several conductive layers with a vacuum hot press.

Figure 1 XXXXXXXXX

Table 1 YYYYYYYYYY

32 mm