Future of Packaging from
No Value-add in the Past to High Value-add in the Future

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The new era of micro- and nano-electronic systems requires that we define and divide packaging into three distinctly different categories: 1) **Semiconductor Packaging** of individual devices; 2) package integration of multiple devices by **2D and 3D Packaging** that cannot be integrated into monolithic devices; and 3) packaging beyond these devices to form highly-functional and miniaturized systems by **Systems Packaging.**

Semiconductor Packaging was defined [1] in the 1980s as interconnecting, powering, cooling and protecting of active devices. Back then, the focus was primarily on devices, since the device scaling and transistor integration was supposed to have led to System-On-Chip (SOC). But that is not the primary focus today as many of the devices such as RF, Optical, Power and MEMS cannot be integrated into CMOS-based mainstream device technology. Packaging, therefore, must address this integration need. Let's call this **2D and 3D Packaging** to interconnect two or more similar or diverse set of devices that cannot be integrated cost effectively into single large SOC chips. This trend started in 1980s when a high performance computing systems required more than 100 similar devices to form a single processor. This led to 2D multi-chip packaging with 100 or more chips interconnected onto a single ceramic or thin film-on-ceramic substrates with lithographic ground rules ranging from 90 microns in thick films to 6 microns in thin films. But systems are more than devices. Only about 20% of systems in volume and cost come from devices. The remaining 80% of the system includes passives, thermal structures, batteries, and interconnection of all these. Let's call this **Systems Packaging.**

Single-chip packaging is the most dominant packaging technology practiced to date starting with lead frame or plastic packaging in the 1970s and moving on to silicon and glass packages in the near future. But its value add at this packaging level to semiconductor companies is minimal, since packaging at a single-chip level adds no benefits either in performance, cost or reliability. It is due to two reasons: to electrically-test the die to guarantee its 100% goodness; and to interconnect the die to other components on the system board by SMT. Packaging at this level can cost more than the device it packages since it involves the package substrate, interconnection, under-fill between the substrate and the die as well as thermal structures. The value-add at this level is very low. For this reason, packaging in the past has been viewed as a necessary evil and single-chip package technology advances have been very cost sensitive and thus are limited.

But new **2D and 3D packaging** is entirely different. It adds value in performance, cost or reliability. It allows new technology advances to be made. Its practice, however, is limited to 2D in high performance systems, since the 1980s and 3-Dimensional SIPs, POPS and more recently to 3D ICs and 3D Interposers. Such an approach dramatically changes the packaging landscape in many ways. For example, with traditional single-chip semiconductor, packaging comes as an after-thought. But in 2D, device and package are co-designed and co-developed so as bring synergy between the two in performance, cost and reliability. The 3D ICs with TSV go a step further, never seen before; they are co-manufactured in the wafer fab even before the back-end of the line I/Os and thus add value to the semiconductor companies.

While the practice of this technology in Fig. 1 is low now, it is expected to grow dramatically.

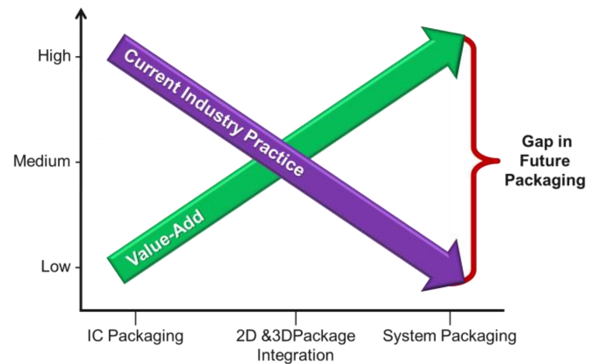

Fig.1 – Current industry practice vs. value-add by three packaging types showing the packaging gap to be addressed in future.

The end goal of any packaging is systems by **Systems Packaging.** The value add is highest but the current practice is lowest. This focus is the next revolution in systems. Since SOC cannot be the basis of this, it is not clear who will drive this next major systems packaging paradigm. It is clear, however, the technology basis for this has to be highly miniaturized actives, passives, interconnections, thermal structures and power supplies, eventually all at nanoscale. Georgia Tech refers to such a technology as 3D All Silicon System (3D ASSM) based on the SOP concept, made possible by ultrathin Si or glass as a system-package, merging the functions of both package and board into one system package. In the past, system companies almost totally depended on advanced semiconductor and packaging technologies from device manufacturers and package integrators but systems packaging had not been their focus and it may never be. They have just migrated to 2D and 3D packaging. Companies like Apple, Sony, Nokia, Samsung, Matsushita, RIM and other consumer electronics companies, however, have both the market need and the financial resources to drive this next revolution to 3D Systems.

References

[1] Rao R. Tummala, and M.Swaminathan editors, ***Introduction to System-On-Package***, McGraw-Hill, 2008.

[2] Rao Tummala, "Moore's Law Meets Its Match," *IEEE Spectrum Magazine*, 43(6), 44-49, 2006.